CHAPTER 4

OPERATION

Section I. CONTROLS AND INDICATORS

4-1. CONTROL AND INDICATOR DESCRIPTIONS. All Remote Control controls and indicators are shown in figure 4-1. Control and indicator functions are explained in table 4-1. The controls and indicators at the Remote Control front panel are identical to those on the 100 Watt Transceiver front panel. With the 100 Watt Transceiver set up for normal operation, pressing push-buttons [2ND] [REMOTE] at the transceiver transfers control to the corresponding controls on the Remote Control. Observe that the REMOTE indicator on the 100 Watt Transceiver illuminates when the REMOTE mode is selected.

4-2. KEYPAD CONTROL. Most control functions are selected via a front panel digital keypad. Keypad selections are entered into memory for use by the microprocessor. The numeric and scroll keys have dual functions. To select the key's second function, the [2ND] key is pressed first, and then the dual function key. Note that when a key or a key dual function is mentioned, brackets are used around the name of the key(s); e.g., [2ND][LOAD] indicates sequential operation of the [2ND] key, then the [LOAD] key.

NOTE

To prevent damage to the keypad use "fingers only" to depress keys.

4-3. OPERATING INSTRUCTIONS. For specific information regarding the operating instructions of the controls and indicators, see section II of this chapter.

Table 4-1. Operating Controls and Indicators

Controls or Indicators	Function
[FREQ]	Used to select an operating frequency.
FREQ Indicator	[FREQ] is pressed, followed by frequency information with numeric keys [0-9], then ENTER. Minimum entry is 01,600.00 KHz. Maximum entry is 29,999.99 KHz. FREQ indicator illuminates only when a frequency is to be entered. Operating frequency of 100 Watt Transceiver is displayed in LCD frequency field.

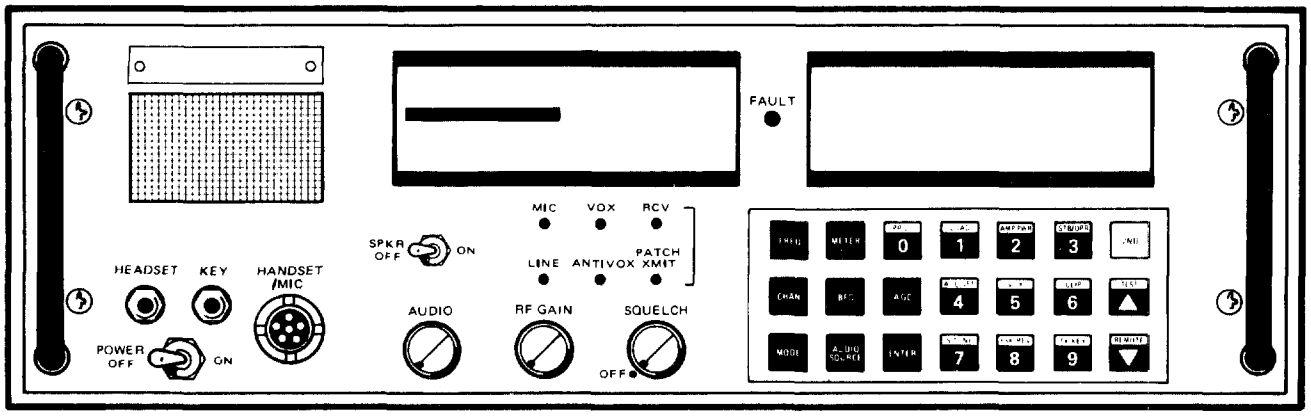

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Figure 4-1. Operating Controls and Indicators

Table 4-1. Operating Controls and Indicators (Continued)

Controls or Indicators	Function
[CHAN] CHAN Indicator	Used to select a 100 Watt Transceiver operating channel. [CHAN] is pressed, followed by channel information with numeric keys [0-9], then [ENTER]. Minimum entry is channel 00. Maximum entry is channel 99. CHAN indicator illuminates when a channel is to be selected or programmed. Operating channel of 100 Watt Transceiver is displayed in LCD channel field (left of frequency display).
[MODE] MODE: USB Indicator MODE: LSB Indicator MODE: AME Indicator MODE: CW Indicator	Used to select and display 100 Watt Transceiver operating mode. Modes are Upper Sideband (USB), Lower Sideband (LSB), Amplitude Modulation Equivalent (AME), and CW (Morse). Press [MODE] to scroll through all four MODE positions. Appropriate MODE indicator illuminates for selected position.
[METER] AUDIO Indicator LINE Indicator PATCH Indicator FWD Indicator REF Indicator VSWR Indicator	Used to select and display Remote Control meter scale. Appropriate scale and units appears on meter display. Meter scales are; "S" (received signal); FWD (forward power); REF (reflected power); VSWR (Voltage Standing Wave Radio); AUDIO (audio source); PATCH (Patch audio source); LINE (Line Audio). Press [METER] to scroll through six meter positions. Appropriate indicators illuminate for selected meter scale.

Table 4-1. Operating Controls and Indicators (Continued)

Controls or Indicators	Function
[BFO] BFO: ON Indicator	Used to select, adjust and display 100 Watt Transceiver Beat Frequency Oscillator (BFO) feature. BFO can be used in detection of all modes except AME. Press [BFO] to select BFO feature. BFO ON (±) shows BFO position in relation to center (no offset). In BFO mode, [SCROLL UP] or [SCROLL DOWN] increments or decrements BFO frequency by 10 Hz per keystroke. There is no readout of BFO frequency. There is no display for BFO off mode.
[AUDIO SOURCE] AUDIO: MIC Indicator AUDIO: AUD2 Indicator AUDIO: PATCH Indicator	Used to select and display audio source. Selections are Microphone (MIC),Audio 2 (AUD 2) and telephone patch (PATCH). Press [AUDIO SOURCE] to scroll through three audio select positions. An indicator illuminates for each AUDIO SOURCE selected.
[AGC] AGC: SLOW Indicator AGC: MED Indicator AGC: FAST Indicator	Used to select and display 100 Watt Transceiver AGC speed (decay). AGC attack time fixed at 30 milliseconds. Decay times are: 3 ±1 second (AGC: SLOW), 200 ±100 milliseconds (AGC: MED) and 30 milliseconds or less (AGC: FAST). Press [AGC] to scroll through three AGC speeds. An indicator illuminates for AGC speed selected. [AGC] does not function if AGC: OFF is displayed (see [AGC OFF]/[4]).

Table 4-1. Operating Controls and Indicators (Continued)

Controls or Indicators	Function
[ENTER]	Used in conjunction with frequency and channel keys to enter information into 100 Watt Transceiver memory.
[PROG]/[0]	Used in programming Channel feature; also used as numeric [0]. Press [2ND] [PROG] to select programming feature.
[LOAD]/[1]	Used with Channel feature to load programming into memory; also used as numeric [1]. Press [2ND] [LOAD] to place channel programming into memory.
[AMP PWR]/[2] LPA MAN Indicator AMP: Indicator	Used to control and display Power Supply status for a companion Linear Power Amplifier (LPA); also used as numeric [2]. Press [2ND] [AMP PWR] to select LPA power supply on and off. LPA must be in AUTO for [AMP PWR] to function (LPA AUTO is selected at LPA front panel). When power supply is on, AMP: STBY indicator illuminates and flashes during 3 minute warm-up period. After warm-up, flashing stops. If LPA is in Manual mode, LPA MAN indicator illuminates, and [AMP PWR] has no effect.

Table 4-1. Operating Controls and Indicators (Continued)

Controls or Indicators	Function
[STB/OPR]/[3] AMP: STBY Indicator AMP: OPER Indicator	Used to control and display Standby or Operate status for a companion Linear Power Amplifier (LPA); also used as numeric [3]. Press [2ND][STB/OPR] to toggle LPA between Operate and Standby conditions. Indication AMP: STBY flashing occurs during 3 minute warm-up period for LPA. Indicator not flashing occurs when warm-up period is over. Any display of AMP: STBY places LPA in bypass and it is transparent to 100 Watt Transceiver operation. Indicator AMP: OPR flashing occurs when LPA is to be tuned. Indicator not flashing occurs when LPA is tuned and ready for operation. The AMP: OPR tune cycle is initiated by keying 100 Watt Transceiver. If AMP: OPER indicator is illuminated and 100 Watt Transceiver is keyed, [STB/OPR] has no effect until keyline is removed.
[AGC OFF]/[4] AGC OFF Indicator	Used to select and display 100 Watt Transceiver Automatic Gain Control (AGC) OFF function. Also used as numeric [4]. Press [2ND][AGC OFF] to turn off AGC operation. When AGC OFF is selected, AGC OFF indicator illuminates. When [AGC] is selected, AGC: SLOW, MED or FAST is displayed, and AGC operation is restored (see [AGC]).

Table 4-1. Operating Controls and Indicators (Continued)

Controls or Indicators	Function
[VOX]/[5] VOX: VOICE Indicator VOX: DATA Indicator	Used to select and display Remote Control Voice Operated Transmit (VOX) feature; also used as numeric [5]. VOX modes are VOX: VOICE, VOX: DATA, and VOX OFF. Press [2ND] [VOX] to scroll through VOX modes. When VOX feature is active, VOX: VOICE OR VOX: DATA indicator illuminates. VOX OFF has no display.
[CLIP]/[6] CLIP Indicator	Used to select and display 100 Watt Transceiver transmit peak audio clipping function (CLIP); also used as numeric [6]. Press [2ND][CLIP] to toggle between CLIP on and off modes. When CLIP on is active, CLIP indicator illuminates.
[S TONE]/[7]	Used to select Sidetone (S TONE) feature; also used as numeric [7]. Press [2ND] [S TONE] to toggle between on and off modes. There is no front panel indicator for sidetone.

Table 4-1. Operating Controls and Indicators (Continued)

Controls or Indicators	Function
[TX KEY]/[9] XMIT Indicator TUNE Indicator	Used to key 100 Watt Transceiver or initiate tune sequence; also used as numeric [9]. Press [2ND] [TX KEY] to toggle keyline on and off. When Transmitter is keyed, XMIT indicator illuminates. If a companion Antenna Coupler is used, TUNE indicator illuminates during antenna coupler tune cycles. At end of antenna coupler tune cycle, TUNE indicator extinguishes. Antenna Coupler tune sequencing is automatic.
[TEST]/[SCROLL UP]	Used to command Built-in Test (BIT) self-test feature; also used as [SCROLL UP]. Press [2ND] [TEST] to initiate receiver self-test feature. At end of a successful test, word "PASSEd" appears in frequency display. Press [2ND] [TX KEY] [2ND] [TEST] to initiate receiver and transmitter self-test feature. At end of a successful test, word "PASSEd" appears in frequency display. If a fault is detected with BIT, frequency display indicates which assembly failed. [SCROLL UP] function is used for frequency, channel and BFO entries.
[REMOTE]/[SCROLL DOWN] REMOTE Indicator	[2ND] [REMOTE] has no function at the Remote Control Unit. REMOTE indicator illuminates in remote mode. There is no indicator for local mode. [SCROLL DOWN] selection is used for frequency, channel and BFO entries.

Table 4-1. Operating Controls and Indicators (Continued)

Controls or Indicators		Function
[2ND]		Used to select second function of dual function keypad pushbuttons. [0] through [9], [SCROLL UP] and [SCROLL DOWN] *have dual functions. Press [2ND] then function to* select.
FAULT LOW PWR BYPASS	Indicator Indicator Indicator	Used to indicate a failure or reduced performance condition. FAULT indicator illuminates when a failure occurs. Press [2ND] [TEST] to reveal source of failure. FAULT light also illuminates when a companion LPA fails. LOW PWR indicator illuminates if RF output power of 100 Watt Transceiver drops below a preset level (nominally 50 Watts). BYPASS is a fault indicator that illuminates when the 100/500 Watt Antenna Coupler is unable to tune. In bypass, the system bypasses the 100/500 Watt Antenna Coupler and is connected directly to the antenna. The Transceiver may transmit in bypass, however, RF power output may be reduced to prevent 100 Watt Transceiver damage.
SPKR	Switch	Used to turn front panel speaker on and off.
AUDIO	Control	Used to set front panel speaker and headset audio level.
POWER	Switch	Used to switch Remote Control primary power on and off.
RF GAIN	Control	Used to vary sensitivity of receiver.
SQUELCH	Control	Used to adjust SQUELCH level allowing only signals exceeding threshold to be monitored.

Table 4-1. Operating Controls and Indicators (Continued)

Controls or Indicators		Function
MIC	Control	Used to adjust microphone preamplifier gain.
LINE	Control	Used to adjust the line output audio level.
PATCH XMIT PATCH RCV	Control Control	Used to adjust patch audio input and output levels.
VOX ANTIVOX	Control Control	Used to adjust Voice Operated Transmit (VOX) feature. VOX adjustment sets threshold of audio level required to trigger VOX keyline output. ANTIVOX adjustment cancels receiver audio output in VOX circuit to prevent false VOX operation.

Section II. OPERATING INSTRUCTIONS

4-4. INTRODUCTION. Operating instructions include only those for the Remote Control. Refer to the technical manuals for any ancillary equipment such as linear power amplifiers and antenna couplers. Since the Remote Control can be operated with a variety of ancillary equipment, it is the responsibility of the user to configure the ancillary equipment to support the intended operations.

4-5. OPERATING SEQUENCES. Individual paragraphs are dedicated to each mode, feature and operating sequence. A summary of the paragraphs is provided below for quick reference. These paragraphs assume the operator is familiar with the information given in section I of this chapter.

Para	Instruction
4-10.	Power Application Sequence
4-11.	Normal Positioning of Analog Controls
4-12.	Control Operation During Periods of Transmit
4-13.	Frequency Selection
4-14.	Channel Selection
4-15.	Mode Selection
4-16.	Audio Source Selection
4-17.	AGC Selection
4-18.	VOX Selection
4-19.	BFO Selection
4-20.	CLIP Selection
4-21.	Sidetone Selection
4-22.	TX Key Selection
4-23.	USB and LSB Operation
4-24.	AME Operation
4-25.	CW Operation
4-26.	Linear Power Amplifier Operation
4-27.	Antenna Coupler Operation
4-28.	Front Panel Adjustments
4-29.	BIT Fault Interpretation
4-30.	Power, VSWR, and Audio Metering
4-31.	Programming of Preset Channels

4-6. SEQUENCING OF CONTROLS. To insure that the equipment is operated properly, follow the paragraphs in the order presented. For example, Mode selection in paragraph 4-15 assumes that the Power Application Sequence has been completed in paragraph 4-10. The Front Panel Adjustments described in paragraph 4-28, and the Power, VSWR, and Audio Metering descriptions in paragraph 4-30 are general to all operations of the 100 Watt Transceiver.

4-7. CONNECTION OF EXTERNAL EQUIPMENT. The connection of external equipment is dependent on the desired configuration.

4-8. EXTERNAL CONNECTIONS. Most applications of the Remote Control require a number of external connections to either the 100 Watt Transceiver or the Remote Control. The following lists the most common:

a. Power source connection.

b. Narrow Band Secure Voice (NBSV) or other audio source to AUD2 port.

c. Telephone line connections (PATCH).

d. Audio connections to external equipment.

4-9. POWER APPLICATION AND WARMUP. The Remote Control is entirely solid state equipment and requires no warmup although up to 30 minutes may be required for stabilization of the frequency standard in the 100 Watt Transceiver. If power is connected to the 100 Watt Transceiver, and the power switch is off, the frequency standard oven is NOT powered. If the 100 Watt Transceiver is used in conjunction with a linear power amplifier, the amplifier requires a period of approximately three minutes for the filaments of the output tube to warm up. During this warm up period, the LPA is in bypass and normal 100 Watt Transceiver operation is allowed.

4-10. POWER APPLICATION SEQUENCE. A sequence for power application is provided below. Operations may commence before the 30-minute frequency standard stabilization period of the transceiver. However, transmit/receive frequency errors (less than 100 Hz) will be experienced until stabilization.

a. Power Application Sequence (100 Watt Transceiver is already turned on).

(1) Turn POWER switch to ON position.

(2) Observe LCD readout contains frequency/mode information present at previous power off;

-or-

Observe LCD readout contains default information:

Frequency	10,000.00 KHz
Mode	MODE: USB
AGC	AGC: SLOW
Audio Input	AUDIO: MIC
Meter	"S" scale (Signal Strength)

(3) Allow 20 minutes for 100 Watt Transceiver frequency standard to stabilize.

(4) Turn on power switch for LPA and Antenna Coupler (if applicable), and select LPA AUTO and Coupler AUTO mode.

(5) Turn front panel speaker switch (SPKR) to ON position.

(6) Press [2ND][TEST]. Observe all front panel LCD segments are turned on, followed by a readout in frequency field indicating "PASSEd". If "PASSEd" readout was not obtained, refer to paragraph 4-32 before proceeding.

b. Normal Settings of Audio Gain, RF Gain, and Squelch Controls

(1) Audio Gain: 1/4 turn clockwise, or adjusted to suit

(2) RF Gain: Full clockwise position

(3) Squelch: Full counterclockwise position into OFF (detent).

4-11. ANALOG CONTROL POSITIONING.

a. Audio Gain. The AUDIO GAIN control affects only the front panel speaker and headset output. The audio outputs available at the rear of the Remote Control have separate level adjustments. If a headset plug is inserted into the front panel HEADSET jack, the front panel speaker is not automatically quieted.

b. RF Gain. The RF GAIN control is typically placed in the high gain position, i.e., the knob is turned fully clockwise. In this position, the RF gain of the receiver is determined by normal AGC action. If a condition exists where normal AGC action is detrimental to reception, the RF GAIN control may be turned counterclockwise. The RF GAIN control then overrides the normal AGC circuit, and manually adjusts the gain of the receiver.

c. Squelch. The SQUELCH control is usually placed into the OFF position, i.e., the knob is turned fully counterclockwise into detent. In this position, all received signals are monitored regardless of strength. If it is desired to monitor only a received signal that is strong enough to rise above the background noise, the squelch function can be enabled. If SQUELCH is desired, the correct setting of the SQUELCH control is found by turning the knob out of detent in the clockwise direction during a period when only background noise is present in the speaker. Turn the SQUELCH control slowly clockwise until the squelch action just mutes the audio output. An incoming signal, above the noise level, will break the squelch and be heard in the front panel speaker. Squelch action affects the audio output to the front panel speaker and headset.

4-12. CONTROL OPERATION DURING PERIODS OF TRANSMIT. Frequency and channel changes can not be made when the 100 Watt Transceiver is keyed. Only the controls [TEST],[S TONE] (no front panel display for Sidetone), [METER] and [CLIP] (not available when Audio Source is AUD2) are active when the 100 Watt Transceiver is transmitting. A keyline inhibit signal prevents equipment damage during the frequency and channel changing operations.

4-13. FREQUENCY SELECTION. Minimum entry is 01.600,00 MHz, maximum entry is 29.999,99 MHz. When operating in the CW mode, an automatic 1 KHz offset is entered in transmitted frequency output. Therefore, for CW-LSB, the actual transmitted frequency is 1 KHz below displayed frequency; for CW-USB, the actual transmitted frequency is 1 KHz above displayed frequency. The select switch for CW-USB/LSB is located on the A1A2 IF Filter Assembly in the 100 Watt Transceiver.

a. Frequency Selection - Numeric Key Method.

(1) Press [FREQ] and observe word FREQ displayed in LCD frequency field.

NOTE

FREQ indicator illuminates only when a frequency is to be entered.

(2) Load desired frequency into display with keypad. Following entry of each number, next digit position blinks.

(3) Press [ENTER] when frequency display is correct.

(4) Observe desired frequency is displayed in LCD frequency field, no digits are blinking, and FREQ indicator is no longer illuminated.

b. Frequency Selection - Scroll Method.

(1) Press [FREQ] and observe word FREQ displayed in LCD frequency field.

(2) Push [SCROLL UP] (also says [TEST]) and observe frequency changes upwards in 10 Hz steps for a brief period and then switches to 1 kHz steps.

(3) Release [SCROLL UP]. Observe frequency display is fixed at some higher frequency.

(4) Press [FREQ] and observe word FREQ displayed in LCD frequency field.

(5) Push [SCROLL DOWN] (also says [REMOTE]) and observe frequency changes downwards in 10 Hz steps for a brief period and then switches to 1 kHz steps.

(6) Release [SCROLL DOWN]. Observe frequency display is fixed at some lower frequency.

(7) Using [SCROLL UP][SCROLL DOWN] keys, select desired frequency.

(8) To Exit Frequency Scrolling Feature, press [ENTER].

4-14. CHANNEL SELECTION. The channel method is used when channels have been preprogrammed with operating frequency and mode (these are the only parameters that can be entered in the channel memory). When the channel feature is not used, the operating frequency and mode are entered individually, starting with the frequency.

NOTE

These instructions assume preset channels have already been programmed. If required, refer to the sequence for programming a preset channel in paragraph 4-31.

a. Channel Selection - Numeric Key Method.

(1) Press [CHAN] and observe CHAN indicator illuminates in LCD channel field.

NOTE

CHAN indicator illuminates only when a channel is to be selected or programmed.

(2) Enter the two-digit channel number into display using keypad. Minimum number is 00; maximum number is 99.

NOTE

Additional digits will re-enter in display allowing correction or re-entry

(3) Press [ENTER] when display is correct.

NOTE

Until [ENTER] is pressed, the 100 Watt Transceiver will be receiving the previous operating frequency without changes.

(4) Observe desired channel is displayed in LCD channel field and CHAN indicator is no longer illuminated.

(5) Frequency and mode will be displayed.

b. Channel Selection - Up/Down Increment Method.

(1) Press [CHAN] and observe CHAN indicator illuminates in LCD channel field.

(2) Push [SCROLL UP] (also says [TEST]) if desired channel is higher than number in display. Channel number now increments higher at one second intervals.

(3) Release [SCROLL UP] when desired channel is displayed.

(4) If desired channel is lower than channel number in display, push [SCROLL DOWN] (also says REMOTE) and observe channel number decrements at one second intervals.

(5) Release [SCROLL DOWN] when desired channel is displayed.

c. To Exit Channel Feature. Press [FREQ] to exit Channel feature.

4-15. MODE SELECTION. For the USB and LSB modes, the carrier is fully suppressed. The AME mode is USB plus carrier, and the CW mode is audio derived with a plus or minus 1 KHz frequency offset. Observe indicator for each mode as follows (AFSK is not available from the Remote Control Unit, even if the option is installed in the 100 Watt Transceiver):

a. USB Upper Sideband

b. LSB Lower Sideband

c. AME Amplitude Modulation Equivalent

d. CW Continuous Wave (Morse)

4-16. AUDIO SOURCE SELECTION. In the CW mode, [AUDIO SOURCE] has no effect. AUDIO: MIC selects audio from microphone connected at front panel HANDSET/MIC jack; AUDIO: AUD2 selects audio via rear panel jack J3; AUDIO:PATCH connects a 2-wire/4-wire telephone circuit via rear panel terminal strip TB1. The internal 2-wire/4-wire hybrid select switch is located on the A4 Audio Interface PWB. The built-in telephone patch may be used with either 2 or 4 wire telephone circuits to permit direct telephone-to-radio communication. The phone patch permits phone line audio to be coupled to the transceiver transmit circuitry and transceiver receive audio to be coupled to the connected telephone line.

NOTE

When connecting to the telephone network, a data coupler unit approved by the applicable regulatory agency (the Federal Communications Commission in the United States) should be used.

Both the incoming and outgoing phone patch audio levels are metered and adjustable via the front panel controls. Selection of two or four wire operation is made via a switch located on the Audio Interface PWB, A4. To access this switch, remove the top cover of the remote control and locate the switch by the assembly. Receive audio will only be present at the PATCH terminals when PATCH is selected as an audio source. The phone patch can accept and can supply audio signal levels from less than -20 dBm to 0 dBm, as adjusted at the recessed front panel controls.

Press [AUDIO SOURCE]. Observe indicators below (must be a voice mode of operation):

a. AUDIO: MIC - Audio Source Microphone. The microphone audio source accepts audio and push-to-talk keyline information from the front panel HANDSET/MIC connector. A compression circuit, in series with this input, will automatically compensate for variations in input levels of ±15 dB. The compression circuit center is set via the front panel MIC adjustment control. The input is designed to be used with a dynamic microphone and carbon type microphones may not be used.

b. AUDIO: AUD2 - Audio Source 2. The Audio 2 source accepts audio and keyline information from the rear panel AUD2 connector (J4). There is no compression circuit associated with the AUD2 input and it is designed to accept a 0 dBm average power speech signal from a 600 ohm source. The sensitivity of the AUD2 input is internally adjusted.

c. AUDIO: PATCH - Audio Source Telephone Patch. The PATCH source accepts audio from the rear panel PATCH terminals. There is no compression circuit associated with this input. The input is designed to accept signals in the range of -20 dBm to 0 dBm.

4-17. AGC SELECTION.

a. AGC OFF Mode. The AGC: OFF mode is used when the gain of the receiver is to be under total manual control with the front panel RF GAIN adjustment. To select the AGC: OFF mode, press [2ND][AGC OFF]. Observe AGC indicator for AGC: OFF. Press [AGC] to exit the AGC: OFF mode.

b. AGC Speed Selection. The AGC characteristic is fast attack and slow decay. The attack time is constant at 20 milliseconds, and decay time is variable at SLOW, MED, or FAST. When a mode of operation (USB, LSB, AME, or CW) is selected, an AGC speed is automatically selected typical for operations in that mode. For example, in SSB voice operations, the AGC:SLOW speed is desired since pauses in speech patterns represent no input signal, and with a slow AGC decay, the AGC is held steady preventing an increase in background noise. To select AGC speed, press [AGC]. Observe indicators for:

(1) AGC: SLOW 3 ±1 second

(2) AGC: MED 200 ±100 milliseconds

(3) AGC: FAST 30 milliseconds or less

NOTE

[AGC] has no effect if the AGC indicator reads AGC: OFF.

4-18. VOX SELECTION. The VOX (Voice Operated Transmit) feature is used to automatically generate a keyline when transmit audio is detected. There is a choice of two VOX attack/decay time constants; one for voice signals, and another for data signals. There are two front panel adjustments for the VOX circuit, the VOX and the ANTIVOX. The VOX adjustment sets the threshold level required to trigger the VOX circuit. The ANTIVOX circuit samples the received speaker audio and applies it out of phase to the VOX circuit. This cancels the effect of the microphone picking up the receive audio signal and prevents false VOX operation. ANTIVOX is adjusted for the acoustical coupling between speaker and microphone, and should be adjusted only when the microphone is in a fixed position. The adjustment procedures for the front panel VOX and ANTIVOX controls are discussed in paragraph 4-31. The VOX feature is selected by pressing [2ND][VOX]. Observe indicators for:

a. VOX VOICE

b. VOX DATA

c. VOX OFF (no VOX indicator)

4-19. BFO SELECTION. The BFO is used to raise or lower the center frequency for the product detector reference in detection of all modes except AME. The rules that apply to the BFO feature are:

a. The BFO function is not used in the AME mode.

b. The maximum BFO offset is ±1000 Hz.

c. There is no display for the BFO frequency. Instead, there is a "BFO ON (+)" indication or "BFO ON (-)" indication. If the BFO is at center frequency, the "BFO ON" indicator is not illuminated.

d. BFO offset is entered with scroll keys with a change of10 Hz per keystroke.

4-20. CLIP SELECTION. The CLIP function is selectable only in the LSB and USB voice modes (not available when Audio Source is AUD2). The feature is used for peak clipping of the transmit audio levels to increase the average RF output levels. The clipper is adjustable internally from 0 dB to 12 dB. The CLIP function is selected by pressing [2ND][CLIP]. Observe indicator CLIP illuminates when clipping feature is selected, and no indicator is illuminated when CLIP feature is not selected.

4-21. SIDETONE SELECTION. The sidetone feature is used to inject a portion of the transmit audio into the receive audio path. This is used for operation in voice modes for headset feedback, and in CW mode for a 1 KHz tone when the CW key is closed, or to monitor the transmit audio during any mode of operation. The sidetone (S TONE) function is selected by pressing [2ND][S TONE]. There is no indicator for sidetone function.

4-22. TX KEY SELECTION. The TX KEY function is selectable in all modes of operation. The feature may be used to generate a keyline whenever the normal keyline is absent, to enable transmit BIT, for test procedures, etc. The TX KEY function is selected by pressing [2ND][TX KEY]. Observe indicator XMIT illuminates when transmitter is keyed. In the CW mode, a CW Key closure is still required to obtain XMIT output power.

4-23. USB AND LSB OPERATION. The single sideband modes, Upper Sideband (USB) and Lower Sideband (LSB), operate with a suppressed carrier. The 3 dB bandwidth of the SSB filters is 350 Hz to 3050 Hz. The procedures to operate in the USB or LSB modes, including all features available to the operator, are found in the following references.

a. Perform POWER APPLICATION SEQUENCE, paragraph 4-10.

b. Perform ANALOG CONTROL POSITIONING, paragraph 4-11.

c. Perform CHANNEL SELECTION, paragraph 4-14, if preprogrammed.

d. Perform FREQUENCY SELECTION, paragraph 4-13.

e. Perform MODE SELECTION, paragraph 4-15, selecting USB or LSB.

f. Perform AUDIO SOURCE SELECTION, paragraph 4-16.

g. Perform AGC SELECTION, paragraph 4-17, default is AGC: SLOW.

h. Perform VOX SELECTION, paragraph 4-18.

i. Perform BFO SELECTION, paragraph 4-19.

j. Perform CLIP SELECTION, paragraph 4-20.

k. Perform SIDETONE SELECTION, paragraph 4-21.

l. Perform LINEAR POWER AMPLIFIER OPERATION, paragraph 4-26.

m. Perform ANTENNA COUPLER OPERATION, paragraph 4-27.

n. Reference FRONT PANEL ADJUSTMENTS, paragraph 4-28.

o. Reference POWER, VSWR, AND AUDIO METERING, paragraph 4-30.

p. Perform TX KEY SELECTION, paragraph 4-22. Use local or remote keyline to transmit.

4-24. AME OPERATION. The AME (Amplitude Modulation Equivalent) operates with carrier and upper sideband. The IF filter for the AME mode is the same filter used in the USB mode, with a 3 dB bandwidth of 350 Hz - 3050 Hz. AME is also known as compatible AM. The procedure to operate in the AME is found in the following references.

a. Perform POWER APPLICATION SEQUENCE, paragraph 4-10.

b. Perform ANALOG CONTROL POSITIONING, paragraph 4-11.

c. Perform CHANNEL SELECTION, paragraph 4-14, if preprogrammed.

d. Perform FREQUENCY SELECTION, paragraph 4-13.

e. Perform MODE SELECTION, paragraph 4-15, selecting AME.

f. Perform AUDIO SOURCE SELECTION, paragraph 4-16.

g. Perform AGC SELECTION, paragraph 4-17, default is AGC: FAST.

h. Perform VOX SELECTION, paragraph 4-18.

i. Perform SIDETONE SELECTION, paragraph 4-21.

j. Perform LINEAR POWER AMPLIFIER OPERATION, paragraph 4-26.

k. Perform ANTENNA COUPLER OPERATION, paragraph 4-27.

l. Reference FRONT PANEL ADJUSTMENTS, paragraph 4-28.

m. Reference POWER, VSWR, AND AUDIO METERING, paragraph 4-30.

n. Perform TX KEY SELECTION, paragraph 4-22. Use local or remote keyline to transmit.

4-25. CW OPERATION. The CW mode (Morse) is full carrier transmission without modulation. A frequency offset of exactly 1 KHz will automatically occur resulting in transmissions 1 KHz above (CW-USB) or 1 KHz below (CW-LSB) the displayed

frequency. The select switch for the CW sideband is located on the A1A2 IF Filter PWB in the 100 Watt Transceiver. The 3 dB bandwidth of the CW filter is ±200 Hz. Typical operation in CW uses the front panel CW KEY jack for connection of a CW keying device. Detection of CW signals assumes the received signal has a 1 KHz offset, and an audio tone of 1 KHz is generated for the front panel speaker without changing the BFO center frequency. If the recovered 1 KHz tone is to be raised or lowered, the BFO feature may be used. The maximum BFO offset is ±1 KHz. There is also a "hang" time circuit (internally adjustable) to allow the transmitter to remain keyed between dots and dashes. After the "hang" time is exceeded, the transmitter will unkey and the received message may be monitored. The procedures to operate in the CW mode are found in the following references:

a. Perform POWER APPLICATION SEQUENCE, paragraph 4-10.

b. Perform ANALOG CONTROL POSITIONING, paragraph 4-11.

c. Perform CHANNEL SELECTION, paragraph 4-14.

d. Perform FREQUENCY SELECTION, paragraph 4-13.

e. Perform MODE SELECTION, paragraph 4-15, selecting CW.

f. Perform AGC SELECTION, paragraph 4-17, default is AGC: SLOW.

g. Perform BFO SELECTION, paragraph 4-19.

h. Perform SIDETONE SELECTION, paragraph 4-21.

i. Perform LINEAR POWER AMPLIFIER OPERATION, paragraph 4-26.

j. Perform ANTENNA COUPLER OPERATION, paragraph 4-27.

k. Reference FRONT PANEL ADJUSTMENTS, paragraph 4-28

l. Reference POWER, VSWR, AND AUDIO METERING, paragraph 4-30.

m. Perform TX KEY SELECTION, paragraph 4-22. Use remote keyline to transmit.

4-26. LINEAR POWER AMPLIFIER OPERATION. The 100 Watt Transceiver may be operated with a 500 Watt or 1000 Watt Linear Power Amplifier (LPA). Complete instructions for LPA operation will be found in the associated LPA manuals. The antenna coupler tuning sequence is automatically integrated with the LPA tuning sequence. If the LPA has been previously tuned at the operating frequency, going from AMP: STBY to AMP: OPER will not initiate another LPA tune cycle. A new LPA tune sequence is initiated when the operating frequency is changed by more than 1%. If the AUTO mode is selected at the LPA, the sequence for placing the LPA into service is as follows:

a. Perform all sequences for features and operating parameters as discussed in preceding paragraphs.

b. Press [2ND][AMP PWR]. Observe indicator AMP: STBY illuminates with the STBY portion flashing.

c. Wait a nominal 3 minutes and observe STBY indicator portion stops flashing. (Waiting period allows LPA final amplifier tube filament to warm up.)

d. Press [2ND][STB/OPR]. Observe indicator now reads, AMP: OPER with the OPER portion flashing (indicating the LPA requires a tune sequence).

e. To initiate a LPA tune sequence, momentarily close the keyline associated with mode of operation, or perform TX KEY sequence discussed in paragraph 4-22. Observe indicator OPER stops flashing when LPA is tuned.

NOTE

This step automatically initiates tune sequence for a companion Antenna Coupler, if used (see paragraph 4-27). When the antenna coupler is tuning, the indicator TUNE illuminates.

f. Remove keyline used to initiate LPA tune cycle; LPA is now ready for normal operations.

g. To place LPA in standby mode, unkey the 100 Watt Transceiver, and press [2ND][STB/OPR]. Observe LPA indicator AMP: STBY illuminates. The LPA is now bypassed and the 100 Watt Transceiver works directly into the associated antenna coupler.

NOTE

If 100 Watt Transceiver is keyed, [STB]/[OPR] has no effect.

h. To deenergize the LPA, press [2ND][AMP PWR]. Observe indicator AMP: STBY is no longer illuminated and LPA is shut down.

4-27. ANTENNA COUPLER OPERATION. There are no direct controls for the 100/500 Watt Antenna Coupler, but there is a control unit associated with the 1000 watt antenna coupler. Complete instructions for the Antenna Coupler will be found in the associated coupler manuals. Operation of the 100/500 Watt Antenna Coupler or operation of the 1000 watt antenna coupler (if placed in AUTO) is completely automatic and requires no special operating sequence. During an antenna coupler tune sequence, the front panel TUNE indicator illuminates. If the 100/500 Watt Antenna Coupler is unable to tune, the indicator BYPASS illuminates. BYPASS indicates that the antenna coupler is bypassed and the antenna is connected directly to the 100 Watt Transceiver/LPA. The 100 Watt Transceiver will transmit when the antenna coupler is bypassed, and automatically reduce transceiver output power to accommodate any encountered VSWR. If the 100 Watt Antenna Coupler, AN/URA-38( ), is unable to tune, it faults and prevents keying until it is tuned. During the tune sequence for the antenna coupler, a much lower RF level is used for tuning. This may cause indicator LO PWR to illuminate, which is a normal occurrence. When the antenna coupler is tuned, full power is applied and LO PWR indications would reflect a genuine low power condition.

4-28. FRONT PANEL ADJUSTMENTS. There are six maintenance controls available to the operator. Each control and its adjustment procedure is discussed below.

a. VOX Adjustments. The VOX feature has two maintenance controls; the VOX threshold and the ANTIVOX threshold. The VOX threshold sets the threshold for the audio level required to trigger the transmitter keyline, and the ANTIVOX sets the threshold for prevention of a keyline during periods of reception.

(1) VOX Threshold Procedure

(a) Connect a microphone to the front panel jack.

(b) Select the VOX feature using the procedure in paragraph 4-18.

(c) Speak normally into the microphone and adjust the front panel VOX adjustment clockwise until the transmitter goes into the transmit mode.

(d) Stop speaking into the microphone and observe the transmitter unkeys after a short delay.

(2) ANTIVOX Threshold Procedure

(a) Tune in a typical radio transmission and adjust the speaker volume for normal listening level.

(b) Select the VOX feature using the procedure in paragraph 4-18.

(c) Connect a microphone to the front panel jack.

(d) Do not speak into the microphone, and adjust the ANTIVOX control counterclockwise until the transmitter keys. When this happens, turn the ANTIVOX control clockwise until the transmitter unkeys. If significant speaker-to-microphone coupling is not present, the transmitter will not key and the Antivox may be left at minimum.

NOTE

There is interaction between the VOX and ANTIVOX adjustments. It may be necessary to conduct these procedures twice, or more, to suit your operational conditions.

b. PATCH Adjustments. The PATCH RCV and PATCH XMIT maintenance controls are used to set the levels to and from the 2-wire or 4-wire external

telephone patch connections, respectively. These controls are set when the audio source is PATCH as follows:

(1) PHONE XMIT Procedure

(a) Establish a phone patch circuit.

(b) Select the front panel meter function AUDIO as described in paragraph 4-30.

(c) Observe the audio peaks on the meter during normal transmission and set the PATCH TX control for voice peaks at 0 dB.

(d) Continue directly to PHONE RCV procedure below.

(2) PHONE RCV Procedure

(a) Select the front panel meter function PATCH as described in paragraph 4-30.

(b) Observe the level of the voice peaks present during normal received conversation.

(c) Adjust the PHONE RCV such that the voice peaks observed in (b) above are -10 dBm. This level may be adjusted upwards if the phone user reports weak received audio.

c. MIC Adjustments. The MIC maintenance control is active when the audio source is MIC. The MIC control adjusts the input transmit audio levels as follows:

(1) Connect a front panel microphone to the equipment.

(2) Select the front panel meter function AUDIO using the procedure in paragraph 4-30.

(3) Press the PTT microphone button and talk normally into the microphone. Observe the audio peaks on the front panel meter.

(4) Adjust the MIC control such that voice peaks register "0" (0dB) on the meter display.

(5) Unkey the transmitter. This completes the procedure. Note that increasing the level above the 0 dB point will not increase RF power but will only cause excessive noise to be transmitted during speech pauses.

d. LINE Adjustments.

(1) Connect the desired termination to the LINE output terminals at the rear of the equipment via TB1.

(2) Select the front panel meter function LINE using the procedure in paragraph 4-30.

(3) Tune in a radio transmission typical for operations and observe the audio peaks on the front panel meter. A steady tone provides the best results.

(4) Adjust the LINE control for the desired level (between -20 dBm to +10 dBm).

4-29 BIT FAULT INTERPRETATION. During system BIT testing, full RF power is generated and appears at the rear panel RF INPUT/OUTPUT jack J1 on the 100 Watt Transceiver. (The transmitted frequency is the frequency entered prior to BIT testing.) To prevent accidental transmissions, or create a hazardous situation, the 100 Watt Transceiver must be keyed to initiate the transmit BIT test sequence. If the 100 Watt Transceiver is not keyed when BIT is selected, only the receiver portion of the 100 Watt Transceiver is tested. If the 100 Watt Transceiver is keyed when BIT is selected, both the receiver and transmitter portions of the 100 Watt Transceiver are tested. Detailed discussions of the BIT fault codes are in chapter 6 of the manual for the 100 Watt Transceiver.

a. BIT Feature Sequence - Receiver Only. Press [2ND][TEST] and observe all indicators illuminate during test, followed by the word "PASSEd" in frequency display.

b. BIT Feature Sequence - Receiver and Transmitter.

CAUTION

Verify the RF OUTPUT jack, J1 at the 100 Watt Transceiver, is terminated into a 100 watt dummy load, or suitable antenna. If a 500 Watt or 1 KW Linear Power Amplifier is connected in the system, verify that its output jack (J5) is terminated into the dummy load or antenna.

Press [2ND][TX KEY][2ND][TEST]. Observe all indicators illuminate during test, followed by the word "PASSEd" in frequency display. Press [2ND][TX KEY] to unkey transmitter.

c. BIT Fault Codes. If a BIT test has detected a fault, an indication of the difficulty will be displayed in the front panel frequency LCD. The faults are coded as listed below:

Display		Fault
1	A1A1	EXCITER
	-0	No Exciter Module installed
	-1	No 455 KHz modulator output
	-3	No 40 MHz modulator USB output
	-4	No 40 MHz AME modulator output
	-5	No 40 MHz modulator CW output
1	A1A2	IF FILTER
	-1	No USB IF
	-2	No LSB IF
	-3	No CW IF
1	A1A3	FIRST CONVERTER
	-1	No 1st Converter receive output
	-2	No 1st Converter transmit output
1	A1A4	100 WATT PA
	-1	No PA output
1	A1A5	LOWPASS FILTER
	-1	LPF band 1 open (receive)
	-2	LPF band 2 open (receive)
	-3	LPF band 3 open (receive)
	-4	LPF band 4 open (receive)
	-5	LPF band 5 open (receive)
	-6	LPF band 6 open (receive)
	-7	LPF latched closed (receive)
	-8	VSWR fault (transmit)
	-9	LPF open (transmit)
1	A1A6	AGC/TGC
	-1	AGC high
	-2	No manual RF gain control
	-3	TGC set point is incorrect
	-4	No TGC action
1	A1A7	RECEIVER
	-0	No Receiver Module installed
	-1	No 2nd Converter receive signal
	-2	Low Receive line level
	-3	Bad Receiver T/R switch (no transmit signal)
	-4	AGC set point is incorrect
1	A1A9	REF/BFO
	-1	BFO unlock
1	A1A10	SYNTHESIZER
	-0	No Synthesizer Module installed
	-1	Synthesizer unlocked
1	A1A12	CONTROL
	-1	Analog/Digital Converter defective
1	A1A13	LPA/COUPLER INTERFACE
	-0	No LPA/Coupler Interface Module installed
1	A1A14	MULTIVOLTAGE CONVERTER
	-1	High voltage
	-2	Low voltage
1	A1A19	REMOTE INTERFACE
	-1	Invalid baud rate
	-2	UART loopback fault
2	Linear Power Amplifier (LPA)	
	-00	No LPA test set by transceiver
	-01	Micro-control fault
	-02	Not used
	-03	Primary power fault
	-04	+13.6V supply fault
	-05	Transmitter fault
	-06	Bandswitch drive fault
	-07	Servo coil drive fault
	-08	High voltage on in standby
	-09	High voltage fault in operate
	-10	Plate current on with bias off
	-11	Plate current fault with bias on
	-12	RF mute not working

	-13	No RF input with Tune Power Request
	-14	Plate current fault when keyed
	-15	No tune peak with RF input power
	-16	Forward power fault
	-17	VSWR/Reflected power fault
	-18	Power gain fault
	-19	Not used
	-20	Auto tune fault (not a BIT code)
	-21	LPA-Transceiver link fault (not a BIT code)
	-22	Plate Current without Forward Power
3		COUPLER
	-01	Coupler fault (not a BIT code)
	-02	Over temperature fault (not a BIT code)
4		REMOTE
	-01	Audio loopback fault
	-02	Invalid baud rate

4-30. POWER, VSWR, AND AUDIO METERING. The metering feature provides for measurement of power, VSWR and audio signals. Selection of each meter feature is discussed below. Press [METER]. Observe that the key scrolls the meter through the following functions and scales:

(1) "S" Received signal strength.

Scale from S3 to +60. This scale is automatically selected when in the receive mode and meter is set to FWD, REF, or VSWR.

(2) AUDIO Transmit audio signal level. Scale from -20 dB to +10 dB. The correct level is 0 dB.

(3) LINE Line audio output signal in transmit. Line input from the 100 Watt Transceiver in receive. Scale from -20 dBm to +10 dBm.

(4) PATCH Patch input (TX) signal when keyed, or Patch output (RX) signal when unkeyed. Scale from -20 dBm to +10 dBm.

(5) FWD TX - Forward power output. Scale from 0 watts to 150 watts. With 500 Watt LPA or 1000 watt LPA, scale is WATTS X 10 (0 watt-1500 watts).

RX - Received signal strength scale from S3 to +60.

(6) REF TX - Reflected power. Scale from 0 watts to 150 watts. With 500 Watt LPA or 1000 watt LPA, scale is WATTS X 10 (0 watt-1500 watts).

RX - (Same as FWD.)

(7) VSWR TX - Voltage Standing Wave Ratio. Scale from 1 (1:1) to 4 (4:1).

RX - (Same as FWD.)

4-31. PROGRAMMING OF PRESET CHANNELS. When using the procedure below, any previous programming of a channel will be displayed. The new information is entered, displacing the previous programming. Only frequency and mode information can be stored in the channel memory. The remainder of the features must be entered manually or the default characteristic will govern, i.e., selecting mode USB automatically selects an AGC speed of AGC: SLOW - if AGC: FAST is desired, this must be entered manually after the channel is selected. After a channel is programmed, the display shows the operating conditions that were set before programming started. The operating parameters of frequency and mode for 100 channels (00 through 99) can be stored in memory. The procedure to place this information into memory is described below:

a. Press [2ND][PROG]. Observe CHAN indicator illuminates.

b. Enter a channel number 00 to 99 with keypad, then press [ENTER]. Observe FREQ indicator illuminates.

c. Enter a frequency 01,600.00 to 29,999.99 with keypad. When frequency is correct, continue to step d.

d. Press [MODE] until desired operating mode is displayed. When mode is correct, continue to step e.

e. Observe desired frequency and mode information is entered correctly; press [2ND][LOAD].

f. This completes programming of a preset channel. Repeat procedure for each channel to be programmed.

Section III. EMERGENCY OPERATION

4-32. CONDITIONS FOR EMERGENCY OPERATION. Under certain emergency conditions, the Remote Control may still be functional with the 100 Watt Transceiver either at full performance or reduced performance depending on the fault. The procedure below details the sequence for emergency operation of the 100 Watt Transceiver from the Remote Control.

a. Difficulty - Ancillary Equipment Failure:

(1) Resolution - Disconnect the ancillary equipment, although for most failures, ancillary equipment automatically goes into a bypass mode and disconnection may not be necessary.

(2) If the 100 Watt Transceiver is used with a 500 Watt LPA and the LPA fails, the LPA will automatically go into a bypass mode. The bypass mode means the input RF power is routed straight through the LPA from input to output. The system will continue to operate normally, with 100 watt transmitter power.

(3) One possible indication of a LPA failure is the illumination of the 100 Watt Transceiver FAULT lamp and the indicator AMP: STBY.

NOTE

Paragraphs (4) and (5) apply to the 100/500 Watt Antenna Coupler only. The 1000 Watt Antenna Coupler, AN/URA-38( ), does not bypass.

(4) If an antenna coupler has failed, the 100 Watt Transceiver is connected directly to the antenna as indicated by the BYPASS indicator. The BYPASS readout means the antenna coupler is unable to tune and has been bypassed. The bypass circuit can handle full RF output levels. In antenna coupler bypass, much of the power applied to the antenna may be reflected due to the impedance mismatch, and the 100 Watt Transceiver or LPA will reduce its output power level for equipment self-protection.

(5) If the failure is not in the antenna coupler, there still may be a BYPASS indication. In this instance, the actual failure (open antenna cable, damaged antenna, etc.) would have to be determined and appropriate action taken.

b. Difficulty - Failure within the 100 Watt Transceiver.

(1) Resolution - Analyze failure and alternatives.

(2) Virtually all 100 Watt Transceiver failures will result in a FAULT indication at the Remote Control front panel. The Built In Test (BIT) feature will identify which fault has occurred as discussed in paragraph 4-29.

CHAPTER 5

THEORY OF OPERATION

Section I. FUNCTIONAL SYSTEM OPERATION

5-1. REMOTE CONTROL FUNCTIONAL OPERATION. Section I provides an overall functional description of the Remote Control at the major component level. Detailed descriptions of Remote Control modules and assemblies are described in section II of this chapter.

5-2. REMOTE CONTROL RECEIVING OPERATION. When the Remote Control is operating with the 100 Watt Transceiver in the receive mode, audio from the 100 Watt Transceiver is passed through Audio Interface PWB Assembly A4. Hybrid transformers on the Audio Interface PWB Assembly convert separate receive and transmit audio to and from a two-wire circuit. This audio is then passed on to Audio/Microprocessor PWB Assembly A2, which implements gain control and may subject the audio to syllabic squelch. The audio signal is then output to either a 3.2 ohm speaker, handset/headset, AUDIO 2, or patch.

5-3. REMOTE CONTROL TRANSMITTING OPERATION. When the Remote Control is operating with the 100 Watt Transceiver in the transmit mode, the input audio is amplified and may be compressed. It is then output on a 600 ohm line to the 100 Watt Transceiver. The input audio is also routed through VOX and ANTIVOX circuitry on the Audio/Microprocessor PWB Assembly, which sends a keyline signal to the Remote Control microprocessor.

5-4. FUNCTIONAL OPERATION AND SIGNAL FLOW OF TRANSMITTING CIRCUITS. For the following discussion of the transmitting circuits, refer to figure 5-1.

a. Transmit Audio Selection. The transmit audio is primarily selected by the front panel AUDIO SOURCE key from one of three sources: MIC audio from a front panel handset/mic, AUDIO 2 audio from an external narrowband secure voice equipment, or PATCH audio from a 2-wire or 4-wire telephone-type circuit. Rear panel connections are used for AUDIO 2 and PATCH audio inputs. A 1.2 KHz audio signal is automatically injected during the BIT self-test sequence.

b. Transmit Audio Level Adjustments. Level adjustments are provided for each of the input audio sources. For a handset/mic connection, the front panel MIC adjustment is used. For a telephone patch connection, the front panel PATCH XMIT adjustment is used. The LINE IN and AUDIO 2 audio lines have internal potentiometers, since the external equipment controls are typically used to set the input level. Each audio source has a stage of amplification or buffering.

c. Transmit Audio Compressor. The selected audio input is sampled by the front panel metering circuit and VOX circuit, and applied to a compressor circuit. The compressor circuit is not under operator control but is automatically enabled ONLY when the MIC audio source is selected. For all other audio sources, the compressor circuit is bypassed. The purpose of the compressor circuit is to equalize varying voice levels so that the audio signal is more uniform in amplitude. The circuit is used only in the MIC audio mode since operations with a microphone can vary substantially from operator to operator, i.e., different operators speak at different voice levels.

d. Transmit Audio Output. The audio signal is output to the 100 Watt Transceiver at rear panel connector TB1. The audio is routed to the 100 Watt Transceiver via a two- or four-wire 600 ohm line. A sample of the transmit audio provides signal level information to the front panel meter display.

5-5. FUNCTIONAL OPERATION AND SIGNAL FLOW OF RECEIVING CIRCUITS. For the discussion of receiver circuits, refer to figure 5-1.

a. Receive Audio Input. Receive audio from the 100 Watt Transceiver arrives at the Remote Control

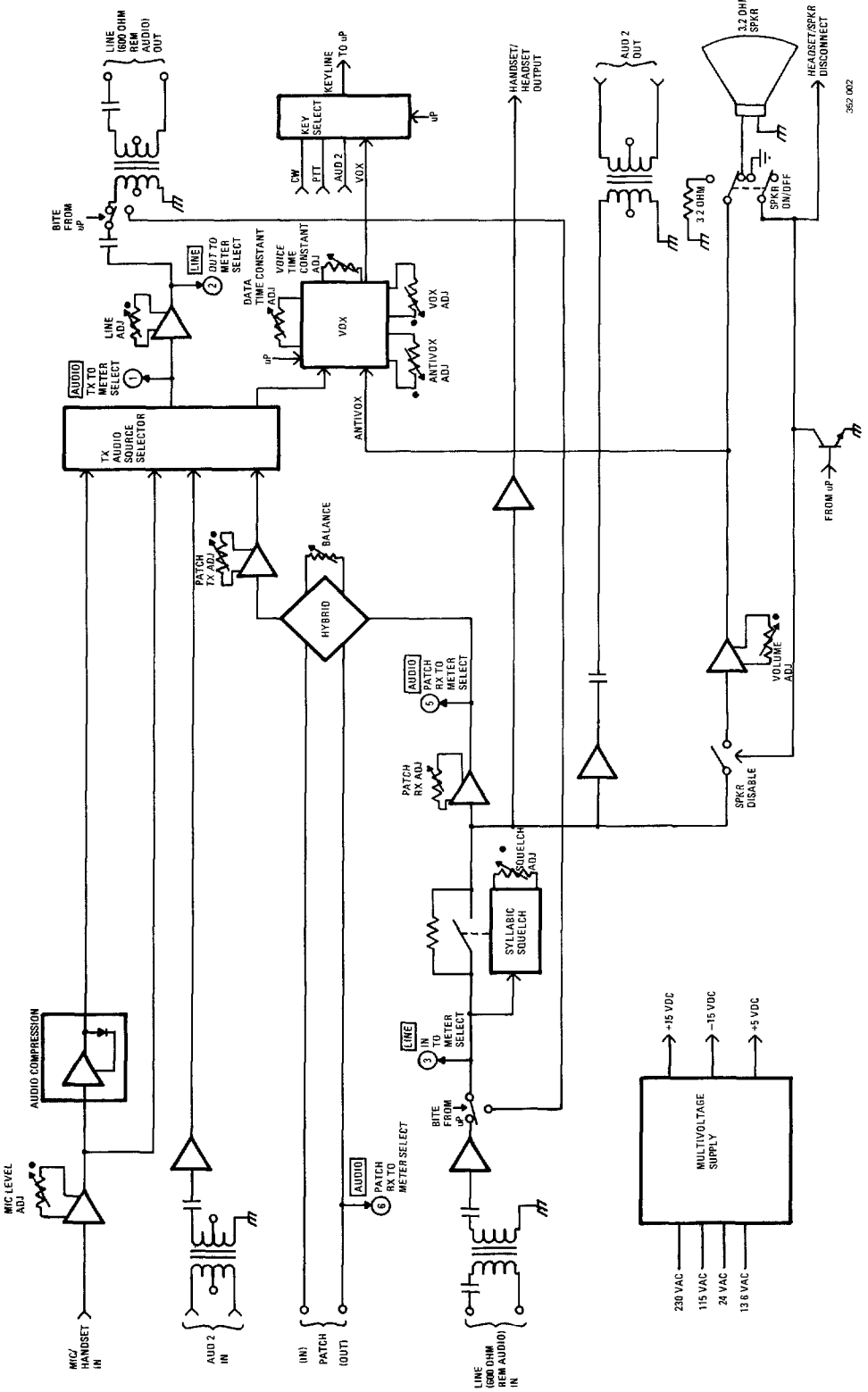


Figure 5-1. Remote Control Simplified Block Diagram (Sheet 1 of 2

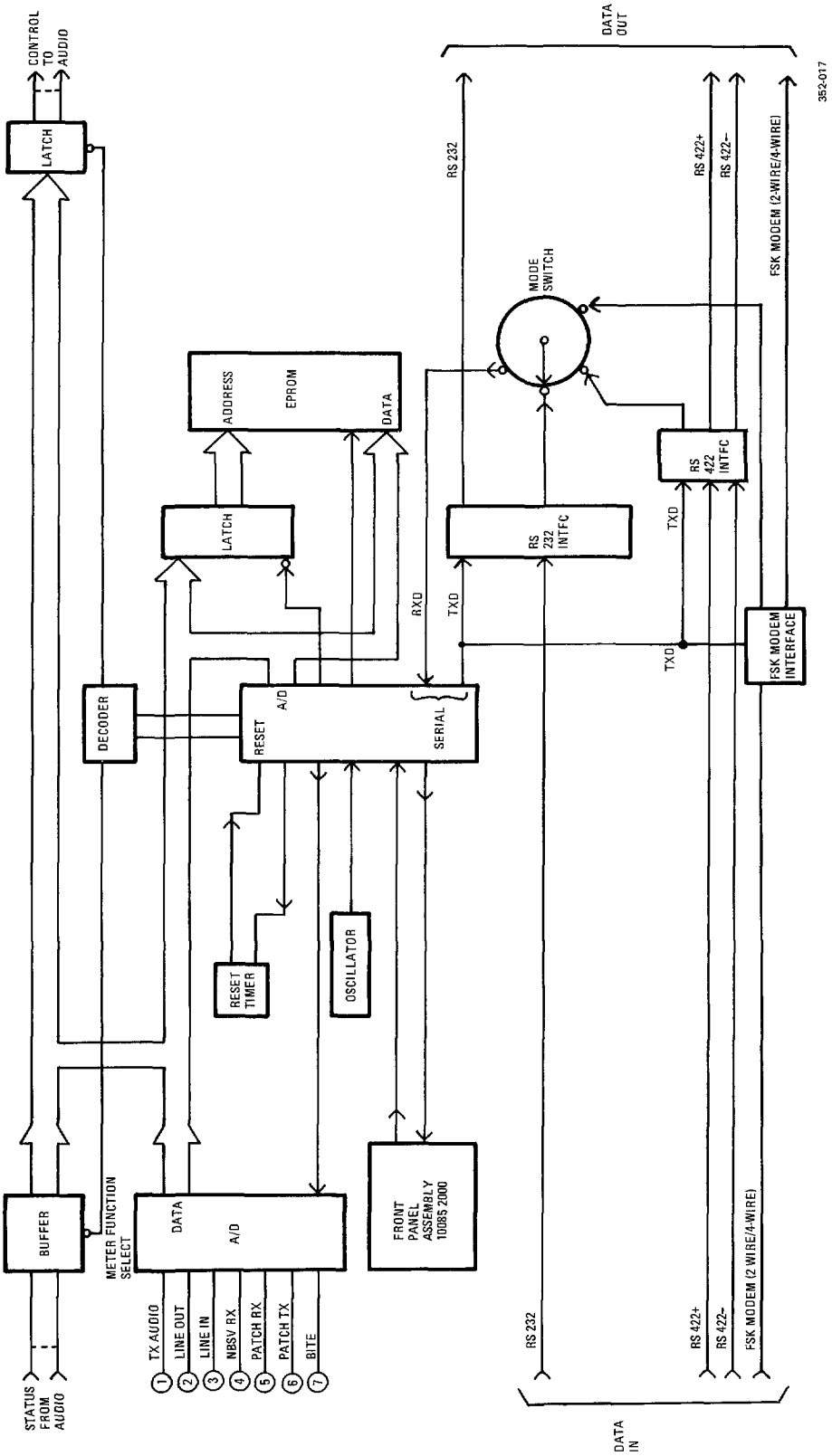


Figure 5-1. Remote Control Simplified Block Diagram (Sheet 2 of 2)

via the 600 ohm line. During the BIT self test sequence, a received signal is simulated at the AUDIO input port, with the normal received signal disconnected for the duration of the BIT test.

b. Receive Audio Squelch. The input audio is sampled by the squelch circuit and metering circuit, and applied to the audio output terminals or front panel speaker after amplification. The squelch feature, which is adjustable and under operator control, is used to mute the audio output when there is no detected audio. Proper squelch adjustment eliminates constant background noise during periods of signal monitoring when nothing intelligible is being received.

c. Receive Audio Level Adjustments. The audio levels are adjustable for the front panel speaker, the LINE output and PATCH receive outputs. The AUDIO 2 output is not adjustable. The squelch feature does not mute the LINE, PATCH, or AUDIO 2 outputs, but does mute the speaker and headset outputs.

5-6. FUNCTIONAL OPERATION AND SIGNAL FLOW OF CONTROL CIRCUITS. The Audio/Microprocessor PWB Assembly is the controlling element for the Remote Control. It monitors the status of the front panel keyboard and directs the activity of the front panel displays. In addition, control and serial data is directed to and from the 100 Watt Transceiver to place the 100 Watt Transceiver in the desired mode of operation. The various activities of the Audio/Microprocessor PWB Assembly are coordinated by the Central Processor Unit (CPU), which in turn follows the program instructions stored in memory.

a. Microprocessor Device. The Central Processor Unit is a type 8031 microprocessor. The 8031 has a 16-bit address bus interface and an 8-bit data bus interface. The address bits A0-A7 are time multiplexed with the data bus D0-D7. That is, terminals AD0-AD7 are sometimes used for addressing and sometimes for data. The CPU resolves the time multiplexing at the beginning of each program bus cycle by first using the AD0-AD7 pins for address, during which the CPU sends out an "Address Latch Enable" (ALE) strobe. The ALE strobe latches the address on lines AD0-AD7 into a device external to the CPU. After ALE, the eight terminals become a 2-way 8-bit data bus for the remainder of the program bus cycle.

b. Permanent Memory. The operating program (software) for the CPU is stored in a Programmable Read Only Memory (PROM) device. The PROM is permanently programmed by the factory and cannot be erased or changed by the user. The PROM has a memory format of 16Kx8, i.e., an input address of 14 bits identifies one of 16,384 locations in memory, the output of which is an 8-bit byte.

c. Temporary Memory. The CPU, in executing the program stored in the PROM, often needs to store data on a temporary basis. Temporary data storage is supplied by a Random Access Memory (RAM) device with a memory format of 2Kx8. An input address of 11 bits identifies one of 2,048 locations in memory. Data is read from a RAM addressed location when the CPU issues a "read" command. Data can be written into the RAM addressed location when the CPU issues a "write" command. There is no non-volatile storage in the Remote Control.

d. Memory and I/O Decoding. The CPU has output control signals "Program Select Enable", "Read", "Write" and "Address Latch Enable". The control signals are combined with address bits to decode memory and Input/Output (I/O) devices. The PROM and RAM are enabled individually by the memory decoding outputs as the CPU does not "see" individual memory devices, but rather, memory as a whole. The same holds true for the I/O devices, of which there are four: Audio I I/O Latch, Audio II I/O Latch, Switch, and Analog/Digital Converter. Through the I/O decoding, the desired I/O port is selected.

e. Microprocessor Reset. CPU program execution is halted and restarted if a "reset" command is generated. "Reset" is generated from any of three conditions:

(1) At power up.

(2) If normal program execution is disrupted.

(3) If manual reset has been activated.

The reset signal is generated by a "Gone-West Timer" circuit. During normal operation of the unit , a reset signal is not generated by this circuit.

f. Analog-to Digital Conversion. The Analog-to-Digital (A/D) element is used for conversion of analog RF GAIN to digital RF GAIN, which is sent to the 100 Watt Transceiver. At the 100 Watt Transceiver, a D/A

device converts the digital signal from the remote control back to RF GAIN analog.

5-7. MULTIVOLTAGE POWER SUPPLY. The multivoltage module has two independent switching power supplies, both powered by a 13.6 Vdc input. The switching power supply, operating at 25 KHz, has an output applied to the switching transformer with a single center-tapped secondary. The switching transformer secondary is full-wave rectified by (+) and (-) diode arrangements, resulting in the +15 Vdc and -15 Vdc outputs. The +13.6 Vdc is also applied to the series-pass switching regulator, resulting in an output of +5.0 Vdc. Inputs and outputs to/from the switching power supplies are passed through an EMI filter.

Section II. FUNCTIONAL OPERATION OF ELECTRONIC CIRCUITS

NOTE

*Indicates that the signal is active low. On schematic diagrams, active low signals have a bar over the top.

5-8. INTRODUCTION. Individual paragraphs are dedicated to each remote control module or assembly. This approach is compatible with the BIT approach to trouble isolation and replacement by assemblies. Text is supported by block diagrams, logic diagrams, timing diagrams and simplified schematic diagrams. These paragraphs assume the operator/technician is familiar with the information given in section I of this chapter. Each module, assembly and sub-assembly in the remote control is assigned a reference designator forming a "family tree" of assemblies. The illustration for the "family tree" is given in drawing FO-1 found in chapter 7. A summary of the reference designators is given in table 5-1.

Table 5-1. Remote Control Assembly Reference Designators

Paragraph		Designation/Assembly
5-10	A1	Front Panel Assembly
5-13	A2	Audio/Microprocessor PWB Assembly
5-16	A3	Multivoltage Supply Assembly
5-17	A4	Audio Interface PWB Assembly
5-23	A1A19	Remote Control Interface PWB Assembly

5-9. OVERALL ASSEMBLY DESCRIPTIONS. The paragraphs in section II follow the sequence in table 5-1. The physical locations of individual assemblies in the remote control are illustrated in figure 1-3. All parts list and component information for the Remote Control is provided in the Depot Manual.

5-10. FRONT PANEL ASSEMBLY, A1. This manual portion describes the Front Panel Assembly as an individual unit. Section I of this chapter describes the function of the Front Panel Assembly in relation to overall Remote Control operation. The Front Panel Assembly, A1, consists of a Front Panel PWB, A1A1, and a Display PWB, A1A2. The following references apply for the detailed discussion that follows:

a. Simplified Front Panel — Figure 5-2

b. Front Panel Assembly Schematic Diagram — Depot Manual

c. Front Panel PWB Schematic Diagram — Depot Manual

d. Display PWB Schematic Diagram — Depot Manual

e. Parts List — Depot Manual

f. Component Layout — Depot Manual

g Overall Interconnection — Depot Manual

h. Remote Control Simplified Block Diagram — Figure 5-1

5-11. OVERALL FRONT PANEL ASSEMBLY FUNCTION. The purpose of the Front Panel Assembly PWB is to provide a readout of 100 Watt Transceiver status signals, functions, frequency of operation, etc. For a discussion of all front panel functions, refer to chapter 4, table 4-1 and figure 4-1. As shown in the simplified functional diagram, figure 5-2, the Front Panel Assembly is essentially a serial-to-parallel shift register with input data loaded serially into the display decoders, and parallel outputs enabling the various display segments. Output data consists of 7 bits of binary

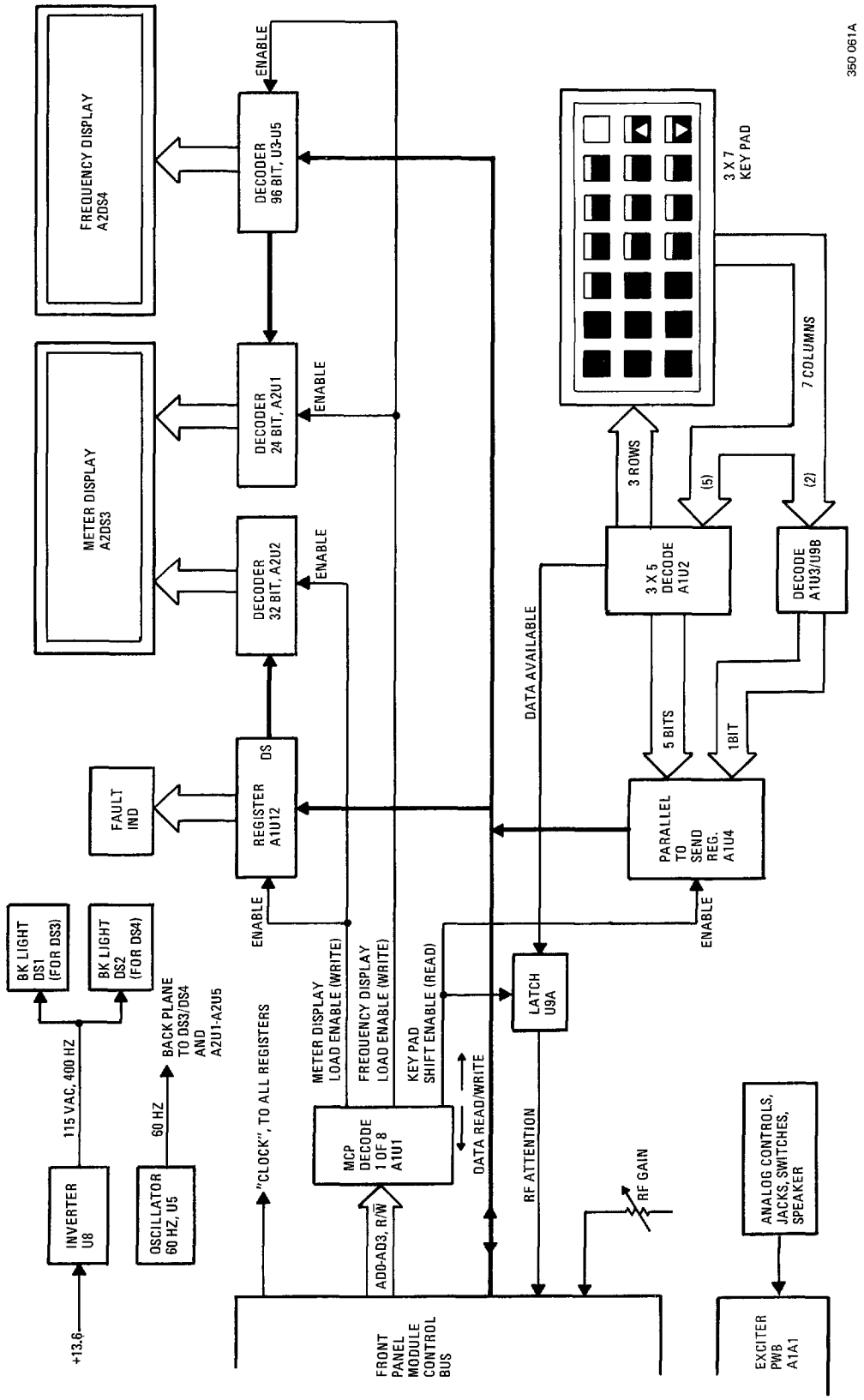


Figure 5-2. Simplified Front Panel PWB

data from the keypad decoder. The remaining circuits support the exchange of data and display devices.

5-12. DETAILED FRONT PANEL ASSEMBLY CIRCUIT OPERATION. For the detailed technical discussion of the Front Panel Assembly, refer to the schematic diagrams located in the Depot Manual. The front panel is the location for all analog controls, digital controls, interconnection jacks, switches, and the audio speaker. All the front panel elements are passive, except for the circuits for the digital keypad and LCD displays. Since the passive devices are readily understood from the schematic diagram, the technical discussion will be limited to the digital keypad and display circuit.

a. Front Panel Module Control Bus Interface Decoding. The FP-MCB interface for the Front Panel Assembly uses only two of sixteen addresses. The control signals for the Front Panel PWB are read into the assembly in a serial data stream. The MCB address strobe consists of two codes, one for the frequency display, and one for the meter display. The AD3-AD2-AD1-AD0 address for the frequency display is 0010 (2); for the meter display it is 0110 (6). Both Read and Write are decoded for the frequency display code, because the keypad readback uses this address, and only a Write function is decoded for the meter display. AD1 and AD0 are used as enables for 1-of-8 decoder U1, and AD3 and AD2 are used as decoder inputs along with the read/write strobe.

b. Meter Display MCB Write Cycle. When MCB data is intended for the meter display, the clock signal clocks serial bits of data into the Front Panel PWB U12-2 shift register port (via inverters U3B/U10D), continuing out of U12-9 and into Display PWB decoder U2. The meter display is associated with a 32 bit register and U12 is associated with an 8 bit register, therefore, for a meter display data write cycle, a total of 40 serial bits are loaded into the associated registers. Display PWB decoder U2 controls meter bar segments and related functions, while only one output of 8-bit register U12-4 is used to illuminate the front panel FAULT indicator. The U1-13 decoded strobe METER LOAD latches the data into the output storage registers of U12 and Display PWB decoder U2, completing a meter display MCB write cycle.

c. Frequency Display MCB Write Cycle. When MCB data is intended for the frequency display, the clock signal clocks serial data bits, via Front Panel PWB inverters U3B/U10D, into Display PWB decoder U3-34. This data is output at U3-35 into decoder U4-34, then into decoder U5-34, and finally into decoder U1-34. This path consists of 32 bits (U3) + 32 bits (U4) + 32 bits (U5) + 24 bits (U1) = 120 serial bits of data for a frequency display data write cycle. Notice that a portion of the meter display is actually serviced by the frequency display data stream. The Front Panel PWB U1-15 decoded strobe FREQUENCY LOAD latches the data into the corresponding output storage registers of the above mentioned decoders, completing a frequency display MCB write cycle.

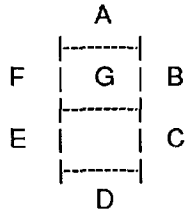
d. Key Shift MCB Read Cycle. Data from the Front Panel PWB back to the Audio/Microprocessor PWB Assembly is via an 8-bit parallel-to-serial converter, U4. During the microprocessor read function, the eight inputs to the parallel/serial register are read in serially to the Audio/Microprocessor PWB Assembly. The key shift strobe is generated from the Frequency Display address, plus the READ strobe at U1-14. The 7 bit inputs to U4 are from the front panel keypad (one U4 bit is not used). Therefore, the readback function of the Front Panel PWB is to route the keypad information back to the Audio/Microprocessor PWB Assembly. Five of the U4 parallel inputs are from the keypad decoder U2. The function of U2 is to decode three rows and five columns of the keypad into a binary output. The remaining two keypad columns (6 keys) are decoded by NAND gate U3, and flip- flop U9B.

e. FP ATTENTION logic generation. When a key is pressed at the Remote Control front panel, the decoding of the selected key is latched into the internal U2 keypad decoder register. Simultaneuously, the U2-13 keypad decoder DATA AVAILABLE (DAV) port is set at logic high. After buffering by U7-B, the logic high clocks both U9A and U9B flip-flop. The clocking of U9A latches a logic high at the U9-5 Q output, which turns on transistor Q1. This places a ground on the FRONT PANEL ATTENTION line. The Audio/Microprocessor PWB Assembly receives this logic low as an interrupt signal and immediately strobes KEY SHIFT to get a readback of the new keypad status. The KEY SHIFT strobe enables the U4 shift register to send back the keypad information, and it clears flip-flop U9A for the next key activation.

f. Display Backlight Circuit. Lighting for the LCD displays is generated by U8. The input to U8 is +13.6 Vdc and the output is 115 Vac, 400 Hz, at 20 milliamperes. The output of U8 is divided into two paths for the two display backlight inputs. U8 is a sealed assembly and not a serviceable item.

g. Backplane Oscillator. An LCD display operates by placing an oscillating voltage on the entire LCD backplane, and then placing the same oscillating voltage, 180 degrees out of phase, on the desired display segment to enable illumination. If the segment has an out-of-phase voltage applied, relative to the backplance oscillator, it illuminates; if the segment has an in-phase voltage applied, it does not illuminate. The backplane oscillator operates at a nominal 60 Hz, and is developed by U5- A/B. It is applied to the display BACKPLANE inputs, and to the display decoder LCD phase inputs. The actual switching of the backplane oscillator is internal to the decoder devices.

h. Display Device Encoding. The schematic diagram for the Display PWB identifies the decoder parallel outputs that illuminate the display segments. To clarify which codes are routed to the segments that form the alpha/numeric characters, refer to the illustration below:



The numbers in the frequency display are counted from left to right, i.e., the channel numbers are 9, 8, and frequency numbers are 7, 6, 5, 4, 3, 2, 1. For example, the segment 4A represents the frequency 10K digit, top segment.

5-13. AUDIO/MICROPROCESSOR PWB ASSEMBLY A2. Section I of this chapter describes the function of the Audio/Microprocessor PWB Assembly in relation to overall Remote Control operation. This part of section II describes the Audio/Microprocessor PWB Assembly as an individual assembly. The following references apply for the detailed discussion that follows:

a. Simplified Audio/ Microprocessor Assembly- Audio Processing	Figure FO-2
b. Simplified Audio/ MicroprocessorAssembly- Microprocessor Control	Figure FO-3
c. Audio/Microprocessor PWB Assembly Schematic Diagram	Depot Manual
d. Parts List	Depot Manual
e. Component Layout	Depot Manual
f. Overall Interconnection	Figure FO-6
g. Remote Control Simplified Block Diagram	Figure 5-1

5-14. OVERALL AUDIO/MICROPROCESSOR PWB ASSEMBLY FUNCTION. The Audio/Microprocessor PWB Assembly has two major sections: audio processing and microprocessor control.

a. Audio Processing Circuitry Introduction. The transmit audio processing circuitry selects the appropriate audio input line, compresses the signal if necessary, amplifies the signal, and directs it to the appropriate output path to the 100 Watt Transceiver. The receive path of the audio processing circuitry receives audio from the 100 Watt Transceiver and provides squelch and volume control before directing it to the headphones or speaker. The audio processing circuitry also implements the front panel gain controls (line, squelch, patch transmit/receive, VOX/ANTIVOX), provides VOX, ANTIVOX and keyline control, and provides data to the front panel meter display.

b. Microprocessor Control Circuitry Introduction. The microprocessor control circuitry includes the microprocessor and interface circuitry needed to control the audio processing circuitry. The microprocessor control circuitry also provides the various interfaces needed to transfer data to and from the transceiver. This circuitry relays front-panel-generated control signals to the audio processing circuitry, which then returns keyline and BIT information to the microprocessor.

5-15. DETAILED AUDIO/MICROPROCESSOR PWB ASSEMBLY CIRCUIT DESCRIPTIONS. The paragraphs which follow describe the Audio/Microprocessor PWB Assembly circuits in detail. Details of the audio processing circuitry are presented first, followed by a detailed discussion of the microprocessor control circuitry. Some description headings include a reference

designator, (e.g. U35, U37, U46) to identify the circuit under discussion. The detailed information assumes the overall Audio/Microprocessor PWB Assembly function is understood from the simplified descriptions provided in earlier paragraphs.

a. Audio Processing. This discussion of audio processing circuitry is divided into the following subtopics: transmit signal flow, receive signal flow, meter function selection, Remote Control BIT, squelch, VOX and ANTIVOX, voice/data time constant, keyline, and power distribution.

(1) Transmit Signal Flow.

(a) Audio Select U35.

1 Three types of audio input devices may be used with the Remote Control: a dynamic microphone, a telephone (patch), or a Secure Voice input device AUD 2.

2 Microphone audio from the Remote Control Front Panel Assembly is input to the Audio/Microprocessor PWB Assembly at pin J5-4. Resistor R65 matches the 150 ohm impedence of the dynamic microphone. Pre-amplifier AR18 supplies gain before microphone audio reaches Audio Select U35 (an analog switching gate).

3 The AUDIO 2 input enters at connector J6 and is applied to transformer T3. The output of T3 enters buffer AR12. The level of the signal is adjustable using potentiometer R51. From AR12 the AUDIO 2 signal is routed to U35.

4 Patch audio enters at pin P4-10 from the Audio Interface PWB Assembly. It then passes through U40A, a variable gain control chip, the gain of which is controlled by a dc voltage (PATCH TX ADJ) at rectifier input pin U40-2. This dc voltage may be adjusted at the PATCH XMIT recessed adjustment on the Remote Control front panel. PATCH TX ADJ enters the Audio/Microprocessor PWB Assembly at pin J9-18. The output at pin 7 of U40 is coupled to U35 by capacitor C90.

5 The switching of U35 is controlled from the Remote Control front panel keyboard. The three audio select control signals (one for each audio source) from the front panel reach U35 via microprocessor U1. A low on one of these lines selects the audio input associated with that control signal as the output of U35.

6 If microphone audio is selected, the microphone signal will pass through U35B to variable gain control chip U40B. The gain of U40B may be adjusted at the MIC recessed adjustment on the Remote Control front panel. The MIC GAIN ADJ line enters the Audio/Microprocessor PWB Assembly at pin J9-15 and is routed to pin 15 of U40. The output of U40 is routed to pin 6 of AR13 via R84 and C142.

7 If either AUDIO 2 or PATCH audio is selected, the appropriate switch of U35 is closed, and the output is connected to pin 6 of AR13 via a resistor.

(b) Final Audio Processing U37, U46, U41

1 The approximately 50 mV_{rms} output of AR13 may be passed through compressor circuitry (U46B) or routed directly to U41B. The path is determined by the audio select lines, which control the state of audio switch U37. In standard configuration of the diode strapping field (pads E1 through E6), the compressor is used only when microphone audio is selected at the Remote Control front panel.

2 At variable gain control chip U41B, gain is controlled by the LINE recessed adjustment on the Remote Control front panel. This adjustment determines the level of the signals that are sent to the 100 Watt Transceiver via the line output. The LINE ADJ dc voltage from the front panel is applied to rectifier input pin 15 of U41 from pin J9-16. The output of U41 passes through amplifier AR14B and encounters BIT-controlled LINE IN/OUT Relay K1. This relay is controlled by a BIT control signal from the microprocessor. Unless a BIT routine is occurring, K1 is closed between pins 2 and 3 and audio is output at LINE OUT pin P4-5 to the Audio Interface PWB Assembly.

(2) Receive Signal Flow. On the Audio/Microprocessor Assembly, receive audio passes through a series of switches (all part of U34), and is picked off at various points along its path to be routed to the four types of output devices that may be used with the Remote Control: speaker, headphones, patch and AUDIO 2.

(a) Line In/Out Switch. Received audio enters the Audio/Microprocessor PWB Assembly at pin P4-7 and passes through the Line In/Out Switch (part of K1). The Line In/Out Switch is held open during the

BIT routine by the BIT control signal from the microprocessor.

(b) Squelch/Keyline Control Switch U34-12,13,14. Following the Line In/Out Switch is the Squelch/Keyline Control Switch (part of U34), which is controlled by the SQUELCH CNTL signal and the KEYLINE IN signal. When the receive audio signal is unsquelched and the 100 Watt Transceiver is not keyed, the Squelch/Keyline Control Switch is closed between pins 12 and 14. During transmit, the receive audio signal path is squelched by opening pins 12 and 14 of U34C, except when BIT is active.

(c) AUDIO 2 Receive. The receive audio signal passes through AR3A, the gain of which is adjusted with AUDIO 2 adjust R59. The resulting signal is then fed to the primary of transformer T4. Outputs of the secondary of T4 are 600 ohm AUDIO 2 RX AUDIO-A (pin J6- 3) and AUDIO 2 RX AUDIO-B (pin J6-2) outputs.

(d) Patch Receive. The receive audio signal is directed to variable gain Patch Rx Gain Control U42. The gain of Patch Rx Gain Control U42 is controlled by the PATCH RCV recessed adjustment on the Remote Control front panel. The output of U42 is fed to PATCH OUT pin P4-9 (via coupling amplifier AR11B, R119, and C108) for patch receive.

(e) BIT Control Switch U34-1,2,15. When BIT is activated, BIT COMMAND at U34-10 goes to logic high connecting U34-15 to U34-1 (ground). This grounds the input of the headphone audio amplifier AR6A and speaker amplifier AR4 removing audio from the headphones and speaker during BIT sequencing.

(f) Volume Control U43. The gain of Volume Control U43 is controlled by the AUDIO control knob on the Remote Control front panel. The VOLUME ADJ signal from the front panel enters the Audio/Microprocessor PWB Assembly at pin J9-12 and presents a dc voltage at rectifier input pin U43-15.

(g) Headphones/Speaker Output. From the BIT-controlled switch (U34), audio passes through amplifier AR6A to Headphones output pin J4-2. Audio also passes through the Handset/Speaker Switch (part of U34), which is controlled by the output of gate U49D. The inputs to U49D are SPKR CNTL from the microprocessor and HANDSET SENSE from the Remote Control Front Panel Assembly and the microprocessor. HANDSET SENSE is hardwired into the circuit, so that it is low when the handset is connected to the Remote Control. SPKR CNTL is under microprocessor control for muting the speaker. When the handset is connected, the Handset/Speaker Switch is held open, and audio does not reach the speaker. When the Handset/Speaker Switch is closed between pins 5 and 4, audio is applied to SPKR OUT pin J4-7 via Speaker Audio Amplifier AR4.

(h) Sidetone Audio. The 50 mV_{rms} transmit audio signal is sampled at pin 15 of U37. This sampled signal passes through amplifier AR13A, the gain of which is adjusted at potentiometer R240. When sidetone audio is selected, the SIDETONE control signal from the microprocessor goes low, and the Sidetone Control Switch (part of U37) closes between pins 14 and 12. As a result, sidetone audio is injected via R241 into the receive path at amplifier AR11A.

(3) Meter Function Select U33. Six analog signals are sampled from the audio processing circuitry and are applied to Meter Function Select U33. U33 is an eight-to-one multiplexer. METER SEL 0 (J7-4), METER SEL 1 (J7-5), and METER SEL 2 (J7-1) control signals from the microprocessor determine which of these six signals is to be read at the meter on the Remote Control front panel. Table 5-2 lists the six signals and the points at which they are monitored. When a signal is selected to be monitored, it is output at pin 3 of U33. The output of U33 is passed through a precision rectifier circuit, consisting of AR5B, CR25, and CR26. A dc level is established at AUDIO MUX output J7-19, which feeds into an A/D device on the microprocessor. The microprocessor sends an eight bit word to the meter on the Remote Control front panel corresponding to the monitored signal level, and the monitored value is displayed.

(4) Remote Control BIT. The Remote Control and the 100 Watt Transceiver have separate BIT circuits, however the results of both tests are displayed at the Remote Control front panel. When the Remote Control BIT routine is completed, it triggers BIT in the 100 Watt Transceiver. During the Remote Control BIT routine, a 1.2 kHz signal from the microprocessor is input at J7-13. The signal is coupled through R71 and C94 to an active low-pass filter (AR12B and associated components). The filter has a cutoff frequency just above 1200 Hz and filters off the harmonics of the 1.2 kHz square-wave input signal. After passing through AR12, the signal is fed

Table 5-2. Signals Monitored by Front Panel Meter

Signal Name	Junction Where Monitored	Input Pin To U33
LINE OUT	R120/R121	1
TX AUDIO	AR13-7/U37-4	5
PATCH TX	C86/P4-10	2
LINE IN	K1-7/R249	13
PATCH RX	R102/R103	15
SPKR	R127/R126	12

into the microphone input at J5-4. This audio test signal is sent through the transmit circuitry, looped back through the receive circuitry, and finally sampled at the patch output.

(a) BIT-Controlled Switches p/o U34, K1.

1 The BIT control signal from the microprocessor affects two switches on the Audio/Microprocessor PWB Assembly to change the signal path. The BIT Control Switch (part of U34) closes between pins 1 and 15 to remove audio from the speaker and headphone outputs during BIT routines.

2 Also during BIT routines, Line In/Out Switch K1 connects line output (K1-2) to line input (K1-7), providing loopback of the 1.2 kHz signal. For K1 to make this connection when BIT has been engaged, the BIT control signal from the microprocessor (via J7-17) goes low. This low is inverted by U48G and applied to pin 7 of U45 and biases on the Darlington transistor array section of U45, which then energizes K1.

(b) Data for BIT Analysis. Data for BIT analysis is acquired at the PATCH RX AUDIO output (P4-9). The signal at P4-9 is divided down by R102 and R103 and then applied to input pin 15 of Meter Function Select U33. During a BIT routine, the divided down PATCH RX output is present on pin U33-3. At the microprocessor, the signal level is compared to a pre-established threshold to determine if the BIT test has passed.

(5) Squelch

(a) Input audio enters the squelch circuit from AR2-1. The signal is passed through a compressor circuit (AR7A, Q2, Q3) and several stages of syllabic rate filtering. If the input signal has sufficient frequency content in the 5 to 18 Hz range, the circuit will detect it and produce output at AR9-7.

(b) A dc input at pin J9-14 from the front panel squelch control establishes a threshold at AR10-3 (via AR9A). The filtered and rectified audio input signal is present at pin AR10-2 and compared to this threshold. If the voltage at pin AR10-2 exceeds the threshold, the output at AR10-1 switches, and the SQUELCH CONTROL signal is applied to pin 11 of the Squelch Control Switch (part of U34). The SQUELCH CONTROL signal causes the Squelch Control Switch to disconnect the audio signal from the subsequent circuitry.

(c) A KEYLINE IN signal from keyline circuitry is connected to pin 11 of the Squelch Control Switch via CR19 and CR50 and will have the same effect as the SQUELCH CONTROL signal. As a result, KEYLINE IN prevents audio from being received while the transmitter on the 100 Watt Transceiver is keyed.

(d) During the BIT routine, a high SQL BYP (Squelch Bypass) signal from the microprocessor (J7-

11) biases Q1 on, which holds the anode of CR18 low. During the BIT routine, the BIT control signal from the microprocessor (J7- 17) is low, which causes the anode of CR19 to be low. As a result of these two inputs, the receive signal path is unsquelched during BIT.

(6) VOX and ANTIVOX.

(a) Each of the three outputs of Audio Select U35 (corresponding to the three types of audio input sources) is connected to pin 2 of AR14 via a resistor (R78, R79, and R80).

(b) The speaker output (J4-7) is divided by resistors R126 and R127 and input to the ANTIVOX circuitry.

(c) The VOX signal is applied to pin 2 of AR16. The output at pin 1 of AR16 is then coupled via capacitor C168 to a variable gain stage (part of U44). The gain of this stage is adjusted at the VOX recessed adjustment on the Remote Control front panel. This front panel adjustment produces the VOX GAIN ADJ signal at J9-20.

(d) The ANTIVOX signal also is capacitively coupled (via capacitor C180) to a variable gain control IC (also part of U44). The gain of this stage is adjusted at the ANTIVOX recessed adjustment on the Remote Control front panel. This front panel adjustment produces the ANTIVOX GAIN ADJ signal at J9-17.

(e) The analog signal at pin 10 of the VOX Gain Control stage is rectified by diodes CR40 and CR41 and filtered by C179. The VOX dc voltage is then directed to R208 via R138. The analog signal at pin U44-7 of the ANTIVOX Gain Control stage is rectified by diodes CR42 and CR43 and filtered by C198. The ANTIVOX dc voltage is then directed to R208.

(f) The VOX and the ANTIVOX signal levels are adjusted at their respective front panel adjusts so that their sum at R208 either exceeds or remains below a pre-set threshold. The threshold is determined by voltage divider R140 and R141 which produces approximately 0.18 V at pin 6 of AR16.

(g) When the audio input intended for keying is strong enough, as determined by the front panel VOX adjust, the VOX dc voltage at R208 will overcome the ANTIVOX dc voltage at R208, and pin 5 of AR16 will exceed the threshold at AR16-6. The output at AR16-7 will switch, charging capacitor C200. The capacitor discharges through potentiometer R195 and resistor R196.

(h) While C200 is charged, the voltage at pin 2 of AR17 will exceed the threshold at pin AR17-3, which is preset by R199 and R200. The normally high output at AR17-6 will go low. This low output is clamped and divided down to approximately 0 V by CR45, R203, and R204, and is applied to pin 12 of an OR gate in U50.

(i) At the other input (pin 13) to this U50 OR gate is the VOX CTL (VOX Control-NOT) signal from the microprocessor (via J7-15). This signal goes low when VOX is selected with the front panel keypad. When VOX CTL is low, the OR gate acts as a buffer and its output is applied to the keyline control logic, which then produces the KEYLINE IN-NOT signal. KEYLINE IN-NOT becomes the primary keying output to the 100 Watt Transceiver via the microprocessor. KEYLINE IN-NOT is also directed to the Squelch Control Switch.

(7) Voice/Data Time Constant.

(a) In addition to the signal from the VOX/ANTIVOX circuitry, the VOICE/DATA CONTROL signal from the microprocessor is input to pin 2 of AR17 via J7-18, U48A, U36A, and R197. When VOICE/DATA is low, the voice time constant is selected, open-collector output pin 2 of voltage comparator U36 is high, and R197 does not conduct.

(b) As AR16-7 goes high and low, the voltage on pin 2 of AR17 is a function of the charge and discharge of C200. R195 and R196 provide a relatively long delay in the discharge of C200, which corresponds to the long decay of voice audio.

(c) When VOICE/DATA CONTROL is high, the data time constant is selected and U36-2 is low. R197, having a much lower resistance than R195 and R196, shunts the capacitor discharge current to U36-2. As a result, C200 has a fast discharge, so that the output at AR17-6 has the fast attack/fast decay desired for data transmission.

(8) Keyline.

(a) The Remote Control has four sources of keying. These sources are listed with the signals they produce and their associated microprocessor control signals in table 5-3.

Table 5-3. Keying Sources

Keying Source	Keying Signal		Associated Control Signal	
	Name	Input Pin	Name	Input Pin
Microphone	PTT KEY-NOT	J5-3	PTT EN-NOT	J7-10
Secure Voice Eq.	AUDIO 2 PTT	J6-1	AUDIO 2 SEL	J7-3
Input from Audio Interface Assembly	EXT KEY-NOT	P4-1	-	-
CW Key	CW KEY-NOT	J5-1	CW MODE	J7-12

(b) The PTT KEY, AUDIO 2 PTT, and CW KEY inputs are paired with their associated control signals into an OR gate of U50. In each case, the control signal goes low when its associated input device is selected. The output of the OR gate associated with CW keyline (U50-6) is inverted by U48 (pins 5 and 4) and is then fed to a debouncing filter circuit, composed of R222 and C201, that eliminates electrical bounce in the keying mechanism. The voltage at C201 is monitored by pin 8 of a voltage comparator (U36C), where it is compared to a 2.5 V reference on pin 9. R227 establishes hysteresis between output pin 14 and input pin 9 to prevent chatter at U36-14. The output at U36-14, CW KEYLINE-NOT, is sent to the microprocessor via J7-14. This signal is also input to a pulse-generating circuit.

(c) The EXT KEY signal is combined with the PTT KEY and AUDIO 2 PTT signals by AND gates U51B and U51D to produce a PTT key signal at U51-6. The PTT key signal is inverted at U48C (pins 7 and 6) and is fed into a debouncing filter circuit composed of R223 and C202. These devices operate just like their counterparts in the CW keyline path.

(d) The output at U36-13 is input to AND gate U51B. The other input to the AND gate is the VOX KEYLINE signal from U50-11. The resulting keyline signal at U51-8 is then input to AND gate U51A.

(e) The other input to AND gate U51A is a SELF KEY-NOT signal from the microprocessor. The SELF KEY-NOT signal allows the microprocessor to initiate keying. The AND gate output at pin 3 is the KEYLINE IN-NOT signal, which is sent to the microprocessor. The KEYLINE IN-NOT signal is also inverted by U48F and used to control the Squelch Control Switch.

(f) The output at U51-8 is also input to a pulse-generating circuit at U49-5. The other input to the pulse-generating circuit is the CW keyline signal from U36-14. The pulse-generating circuit consists of two exclusive NOR gates (U49) with a delay circuit (R232 and C204) at one input of the second gate. The delay circuit is used to produce a negative-going pulse at output pin U49-10 in response to level changes. The output, KEYLINE INTERRUPT-NOT, is sent to the microprocessor via J7-2. This signal informs the microprocessor when keying or unkeying occurs so that it may respond to this high priority function. When either the PTT keyline signal, KEYLINE IN-NOT (at J7- 9), or the CW keyline signal, CW KEYLINE-NOT (at J7-14), go low, the microprocessor is informed that the 100 Watt Transceiver is to be keyed.

(9) Power Distribution. Control cable W1 routes ±15 Vdc and ground to the Front Panel Assembly for reference in the front panel adjust circuits. W2P2 from J8 applies power to the Front

Panel Assembly with the ±15 Vdc and +5 Vdc that arrive at J3 from the Multivoltage Supply Assembly. Zener diode CR39 and R115 develop approximately -5 Vdc from the -15 Vdc input. The ±15 Vdc and ±5 Vdc are distributed to circuits on the Audio/Microprocessor Assembly.

b. Microprocessor Control. This discussion of the microprocessor control circuitry is divided into the following subtopics: microprocessor reset, clock generation, microprocessor control/front panel interface, microprocessor interrupt, address and data lines, microprocessor memory, input/output from/to audio processing circuitry, BIT Oscillator, analog-to-digital (A/D) conversion, data interface, BAUD rate selection, and voltage regulation.

(1) Microprocessor Reset U27, U3.

(a) When pin 9 (RST) of Microprocessor U1 is held high, the microprocessor is held in the reset mode. When pin 9 goes low, the microprocessor is enabled. The state of pin 9 may be controlled by either a manual reset or an automatic reset. Each of these reset controls may be jumpered to an input of NAND gate U27. The output of U27 is connected to U1-9.

(b) Input pin 8 of U27 is normally held high (+5 V), deferring reset control to input pin 9. To manually reset the microprocessor (for testing), a jumper is connected between E19 and E20, pulling U27-8 low. This low is inverted to a high on output pin 10, and the microprocessor is put in the reset mode.

(c) During normal operation, a jumper is connected between E17 and E18; and the E19/E20 junction is left open. In this configuration, reset of the microprocessor is controlled by "Gone-West Timer" U3. Inputs D0 through D7 to U3 are all tied high (+5 V) except input D3, which is grounded. U3 acts as a continuous counter, with serial output at Q7, pin 9, which would count down from bit D7 (pin 6) to bit D0 (pin 11) were it not inhiBITd by a PL (Parallel Load) command from output port P3.4 (pin U1-14).

(d) When the microprocessor is functioning properly, it toggles the PL signal before U3 has counted down to the only grounded bit (D3, pin 14). As a result, output pin U3-10 (DS) remains high, and the RST input (pin U1-9) remains low. The microprocessor is not reset.

(e) If the microprocessor fails to inhibit U3 before it clocks out D3, indicating a malfunction, the low on D3 reaches the input to U27, and the RST input to the microprocessor goes high. The microprocessor is reset.

(f) During powerup R38 and C54 hold pin 10 of U27 low for approximately one time constant in order to keep the microprocessor reset while Powering-Up

(2) Clock Generation Y1, U4, U5, U6, U29.

(a) The clocks required by the microprocessor control circuitry are derived from the 4.9152 MHz crystal Y1 in conjunction with U4. The 4.9152 MHz signal is input to the microprocessor at pin 19 (XTAL 1) and is also divided down by parallel counters U6 and U29 for generation of other clock frequencies. Before the output of the crystal oscillator may be input to U6, it must be divided down by a flip-flop on U5 so that it is below the approximately 3.5 MHz limit of CMOS devices. The approximately 2.5 MHz signal from U5-5 is used on ripple counter U6 to generate a 614.4 KHz signal at pin U6-7 (Q2), a 153.6 kHz signal at pin U6-5 (Q4), a 2.4 kHz signal at pin U6-14 (Q10), and a 600 Hz signal at pin U6-1 (Q12).

(b) The 614.4 kHz signal is used as the clock on A/D Converter U18. The 153.6 kHz signal is input to pin 15 (T1) on the microprocessor to clock two internal counters (see next paragraph). The 2.4 kHz signal is input to another flip-flop on U5 (at pin 11) to generate a 1.2 kHz signal for BIT. The 600 Hz signal is input to pin 10 of ripple counter U29, which then generates an 18.75 Hz signal at output pin U29-3 (Q5) to be used as the clock on "Gone-West Timer" U3.

(c) The microprocessor has two internal counters, which use the 153.6 kHz clock at pin U1-15 (T1): a programmable real-time clock used for time-delays, etc. and a counter dedicated to the on-chip UART. The programmable real-time clock is set for 2 msec intervals. The counter is used for BAUD rate generation for asynchronous data transmission. 9600 to 300 BAUD rates are supplied to interface between the Remote Control and the 100 Watt Transceiver.

(3) Microprocessor Control/Front Panel Interface J2. Connector J2 interfaces between microprocessor programmable ports P1.0 through P1.6 and the Front Panel Assembly. Ports P1.0

through P1.6 are programmed as either inputs or outputs to the microprocessor. Port P1.1 is programmed as both input and output and carries serial data to and from the microprocessor. The R/W (Read/Write) output at port P1.4 determines the direction of data transmission on the data line. Port P1.0 is strictly an output port and transmits the clock pulse generated on the microprocessor to the Front Panel Assembly. Ports P1.2 (FP ADDR 2) and P1.3 (FP ADDR 3) are the strobe outputs from the microprocessor that are used to access modules on the Front Panel Assembly.

(4) Microprocessor Interrupt. The ATTN line at pin J2-5 goes low when a key is pressed on the front panel keyboard. This signal passes through U8A to the INT 1* input (pin 13) on the microprocessor. A low input INT 1* interrupts the microprocessor. The other interrupt to the microprocessor is the KEYLINE INTERRUPT*, generated on the audio processing circuitry and input to the microprocessor at the INT 0* input (pin 12). A SELF KEY* command is generated at microprocessor output port P1.7 in response to pressing the front panel transmit key. This SELF KEY* is routed directly to the audio processing circuitry.

(5) Address and Data Lines. The microprocessor accesses devices in the microprocessor control circuitry via a 16-bit address bus, and data is transferred to and from the microprocessor via an 8-bit data bus. The lower eight bits (A0 through A7) of the address bus (A0 through A15) share lines with the data bus (D0 through D7). Because address and data are on the same eight lines, Low Order Address Latch U7 is needed to demultiplex the data from the low-order address lines. When the microprocessor is addressing a device, it issues an Address Latch Enable (ALE) command, which enables U7. Low order address bits A0 through A7 are then latched through to the U7 output pins.

(6) Microprocessor Memory. The microprocessor may access two types of memory: program memory and data memory.

(a) Program Memory U12. Program memory is stored in U12, a 16 K x 8 bit EPROM (Eraseable Programmable Read Only Memory). Address lines A0 through A13 select memory locations in program memory when U12 is enabled. U12 presents the data (D0 through D7) from the selected memory location to the address and data bus (AD0 through AD7). U12 is enabled by address lines A14 and A15 via Program Memory Decoder U30.

(b) Program Memory Decoder U30. Address lines A14 and A15 are input to the A0 (pin 1) and A1 (pin 2) inputs of 3-to-8 line Program Memory Decoder U30. (The A2 input at pin U30-3 is grounded.) U30 decodes the two address bits to produce an output at pin U30-15. If EPROM U12 is to be enabled, the output at U30-15 will go low. To decode A14 and A15, U30 must be enabled by a low PSEN signal from pin 29 of the microprocessor. This command prevents simultaneous access to program and data memory, because data memory can be accessed only when the PSEN output is high.

(c) Data Memory U25. Data memory is stored in U25, a 2 K x 8 bit CMOS RAM (Random Access Memory). Address lines A0 through A10 select memory locations in data memory when U25 is enabled. Data (D0 through D7) may then be read from or written into the selected memory location via the address and data bus (AD0 through AD7). U25 is enabled by address lines A11, A12, and A13 via Data Memory Decoder/Device Select U13. Low-true RD (Read) and WR (Write) commands, issued by the microprocessor, configure U25 to either write data onto or read data from the data bus.

(d) Data Memory Decoder/Device Select U13. Address lines A11 through A13 are presented to the A0 through A2 inputs of 3-to-8 line Data Memory Decoder/Device Select U13 and decoded to one of five outputs (pins U13-11 through U13-15). These low-true outputs are: RAM SEL, ADC, AUDIO 1, AUDIO 2, and SW. A low RAM SEL output enables RAM U25. The other outputs of U13 will be discussed in later paragraphs. U13 is enabled by a high PSEN command from the microprocessor.

(e) RD and WR Control Lines. The microprocessor uses the low-true RD and WR control lines to indicate whether data is to be read from or written to RAM U25 (as well as A/D Converter U18, output devices U17 and U14, and input device U19, all to be discussed later). To read data from the RAM, the RD* output at pin U1-17 is pulled low, while the WR* output at pin U1-16 remains high. To write data into the RAM, the WR* output is pulled low, while the RD* output remains high. The WR* and RD* lines are input to pins 4 and 5 of AND gate U8B. The output of this gate (at pin U8-6) will be low when the microprocessor is writing or reading and is used as the second enable inputs to U13 and U25. The WR* line

is also input to AND gate U8C with +5 V at the other input. The buffered WR* signal at output pin U8-8 is presented to the R/W* (Read/Write*) input at pin U25-21 and configures the RAM to either write data to (R/W* low) or read data from (R/W* high) the address and data bus.

(7) Input/Output from/to Audio Processing Circuitry U17, U14, U19.

(a) The microprocessor communicates with the audio processing circuitry on the other half of the assembly via connector J7 on the paddle board mounted at the center of the assembly (P3). All lines between the microprocessor control circuitry and the audio processing circuitry, except the SELF KEY* line, pass through J7. These lines, except the SELF KEY*, AUDIO MUX, and KEYLINE INTERRUPT* lines, are latched into or out of the microprocessor control circuitry by latches U17, U14, and bus transceiver U19.

(b) The output control lines to the audio processing circuitry (except the SELF KEY line), are latched by Output Latch U17 and Output Latch U14. To enable U17, the WR command (from the microprocessor) and the AUDIO 1 select signal (from output pin U13-13) are input to NOR gate U15C. If both WR and AUDIO 1 are low, NOR gate output pin U15-10 is high, and U17 is enabled. The AUDIO 2 select signal (from pin U13-12) and the WR command enable U14 via NOR gate U15D.

(c) In addition to lines to J7, U17 also latches out the Analog Loop Back (ALB) line to FSK Modem U22. The functions associated with the other lines latched out by U17 and U14 are explained in the discussion of the audio processing circuitry.

(d) The lines that are input to the microprocessor from the audio processing circuitry, except the KEYLINE INTERRUPT* and AUDIO MUX lines, are buffered by bus driver U19. The functions associated with these input lines are explained in the discussion of the audio processing circuitry. U19 also buffers the End Of Conversion (EOC) signal from A/D Converter U18 and the output of BAUD Rate Select Switch S3 into the microprocessor control circuitry.

(e) To enable U19, the RD command (from output pin 17 of the microprocessor) and the SW select signal (from output pin U13-11) are input to NOR gate U32A. The output of this gate is input with ground to NOR gate U32B. The output of U32B (at pin U32-4) is a low-true enable to U19. When both RD and SW are low, U32-4 is low, and U19 is enabled.

(8) BIT Oscillator U5. The BIT circuitry sends a 1.2 kHz signal through the transmit and receive paths of the audio processing circuitry. This 1.2 kHz signal is developed from the 2.4 kHz output at pin 14 of ripple counter U6, which is input to pin 11 of flip-flop U5. Reset pin 13 of U5 is normally high, holding the flip-flop in the reset mode so that the 1.2 kHz signal is not generated. When the microprocessor issues a BIT command, the data lines produce a low at output pin 2 of Output Latch U17. This low, in addition to being output as the BIT control signal to the audio processing circuitry, is inverted by a NAND gate on U27. A high is then presented to reset pin U5-13. When pin 13 goes high, the reset function is inhiBITd, and the flip-flop divides the 2.4 kHz input to a 1.2 kHz square- wave output at pin 9. This square-wave is then output to audio processing circuitry, where it is converted to a sine-wave and input to the transmit path.

(9) Analog-to-Digital (A/D) Conversion U18.

(a) A/D Converter U18 converts the analog RF Gain In signal from the Front Panel Assembly (via J2) and the analog AUDIO MUX signal from the audio processing circuitry (via J7) to digital signals on data lines AD0 through AD7. Address lines A0 through A2 select which analog signal is to be read. The clock input (pin U18-10), from pin 7 of parallel counter U6, sets the sampling time of U18 at 614.4 kHz.

(b) The low-true WR control and ADC select signals are input to NOR gate U15B. When one of the analog signals is to be converted, both of these lines go low, and the NOR gate output (pin U15-4) places a high on the START and ALE input pins to U18. A high on the START input signals the A/D Converter to start conversion. A high on the ALE (Address Latch Enable) input latches in the three address bits on pins U18-23 through U18-25.

(c) When the analog data has been written into U18 and conversion is completed, the EOC (End Of Conversion) output pin U18-7 goes high. The EOC signal is fed back to the microprocessor via bus driver U19. The ADC select signal is also input to NOR gate U15A with the low-true RD signal. When both of these signals are low, a high is placed on OE (Output Enable) pin U18-9, and the digital information is latched onto data lines AD0 through AD7.

(10) Data Interface. Transmit and receive data passes between the Remote Control and the 100 Watt Transceiver via data interface circuitry on the Audio/Microprocessor PWB Assembly. Three types of data interfaces are provided: FSK Modem (Bell 103 Standard), RS 422, and RS 232.

(a) Interface Select Switch S4. Interface Select Switch S4 is set to position 1, 2, or 3 to select either the RS 232, RS 422, or FSK Modem interface for receive data. Position 4 is used to loop back the receive data into the transmit path for testing purposes.

(b) FSK Modem.

1 Two/Four-Wire Operation Switch S5. Two/Four-Wire Operation Switch S5 configures the FSK Modem interface for either two-wire or four-wire operation. In two-wire operation, transformer T1 handles both transmit and receive data. In four-wire operation, T1 handles the transmit data, and transformer T2 handles the receive data.

2 FSK Modem U22. 300 BAUD FSK Modem U22 has filter and modem circuitry to convert serial input to the audio tones required for FSK Modem signaling. Transmit data from the microprocessor is input at pin U22-10 and output at pin U22-16 to op-amp input AR1-2. This op-amp presents the generated FSK transmit frequencies to T1, which then outputs the FSK data to the 100 Watt Transceiver via connector J1. Receive data from either T1 (two-wire operation) or T2 (four-wire operation) is input at pin 5 of op-amp AR1B, which then presents the receive audio FSK data to pin 15 of FSK Modem U22. U22 converts the audio FSK data to serial data and sends it (via pin U22-4) to pin 13 of AND gate U8D, along with the inverted (via U32C) DCD (Data Carrier Detect) signal from pin U22-2. The DCD signal at pin U22-2 goes low when a valid carrier frequency is detected on the incoming receive data. The DCD signal then allows FSK receive data to pass through U8D, from which it is routed (via S4) to the RXD (Receive Data) input (pin 10) to the microprocessor. An ALB (Analog Loop Back) command may be generated at the microprocessor and input to pin 1 of U22. The ALB command configures U22 to loop transmit data back to the FSK receive data path, converting the transmit data to the appropriate receive frequencies. This feature tests operation of FSK Modem U22 when Interface Select Switch S4 is in the FSK position.

(c) RS 422. Transmit data from the microprocessor is input to U9 for conversion to bipolar RS 422 data at outputs J1-4 (+) and J1-16 (-). RS 422 receive data enters the Audio/Microprocessor PWB Assembly at pins J1-9 (+) and J1-20 (-). These lines are input to pins 6 and 7 of U26. The output of U26 is then relayed to the RXD input to the microprocessor via S4.

(d) RS 232. Transmit data for the RS 232 output is inverted by line driver U10A and output at J1-2. RS 232 receive data is inverted by a line receiver U16A and relayed to the RXD input to the microprocessor via S4.

(11) BAUD Rate Selection. BAUD rate for asynchronous data transmission is selected with rotary switch S3, which inputs to Input Latch U19. Table 5-4 shows the switch positions corresponding to the various BAUD rates. The BAUD rate selection information is sent to the microprocessor via the data bus, where the appropriate BAUD rate is generated by an internal counter.

(12) Voltage Regulation VR2 and VR5. Voltage Regulator VR2 develops -5V from the -15 V line. The -5 V is used for the FSK Modem interface circuitry. Voltage Regulator VR5 develops +12 V from the +15 V line. The +12 V is used for FSK Modem interface circuitry.

5-16. MULTIVOLTAGE CONVERTER ASSEMBLY A3. The following references apply for the detailed discussion that follows:

a. Simplified Multivoltage Converter Assembly	Figure FO-4
b. Simplified Push-Pull Pulse -Width Modulating Regulator	Figure 5-3
c. Simplified Series-Pass Pulse -Width Modulating Regulator	Figure 5-4
d. Multivoltage Converter Assembly Schematic Diagram	Depot Manual
e. Parts List	Depot Manual
f. Component Layout	Depot Manual
g. Overall Interconnection	Depot Manual

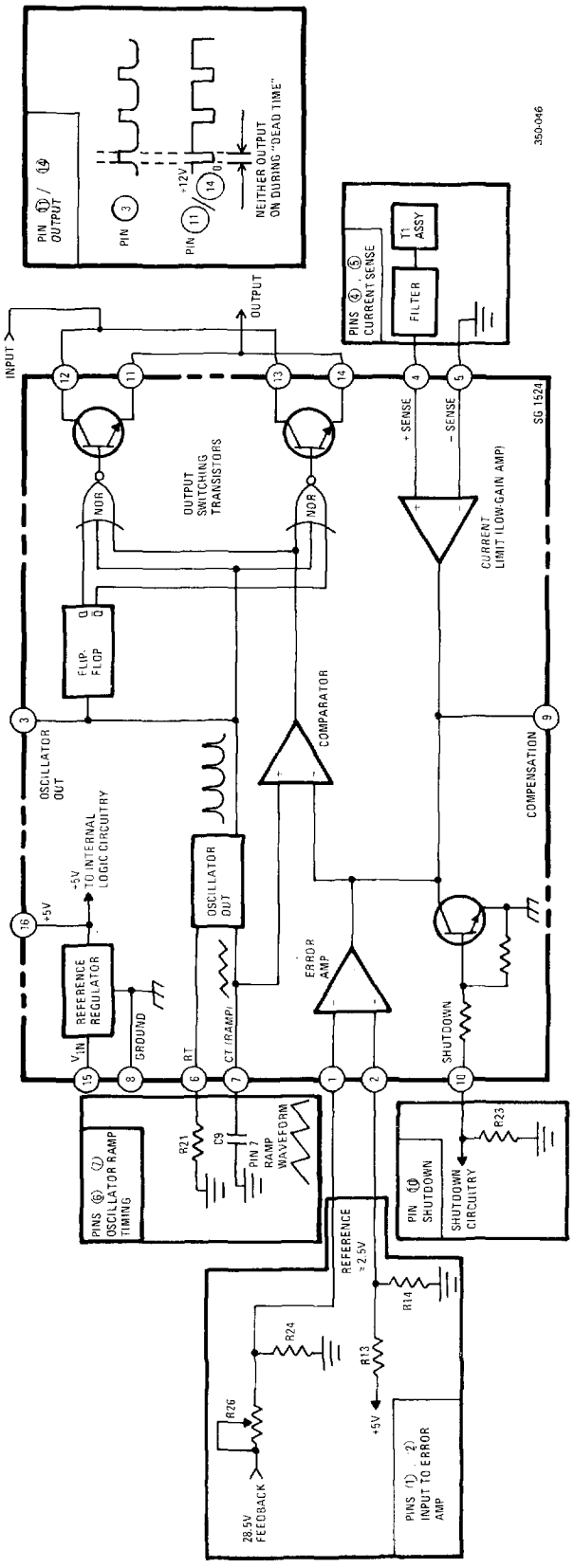


Figure 5-3. Simplified Push-Pull Pulse-Width Modulating Regulator

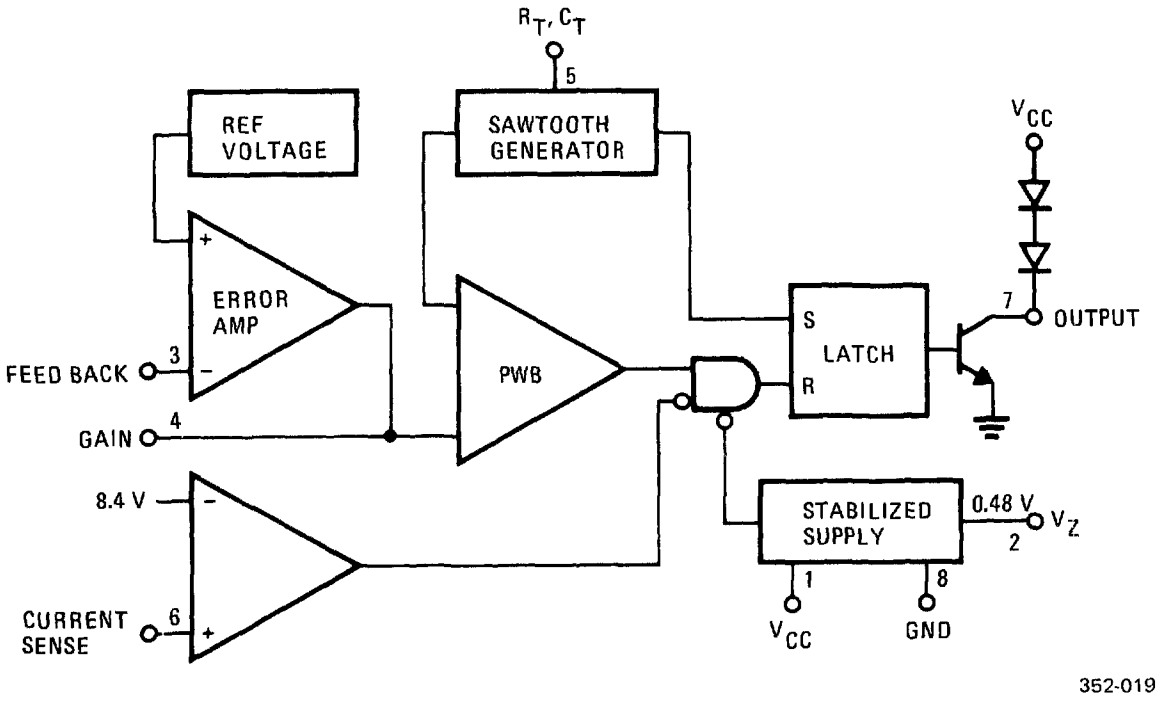


Figure 5-4. Simplified Series-Pass Pulse Width Modulating Regulator

Table 5-4. BAUD Rate Selection

Switch Position	BAUD Rate
0	300
1	600
2	1200
3	2400
4	4800
5	9600

h. Remote Control Simplified Block Diagram Figure 5-1

a. Overall Multivoltage Converter Assembly Function.

(1) Multivoltage Converter Assembly A3 is identical to the Multivoltage Converter Assembly in the 100 Watt Transceiver and consists of two subassemblies: Multivoltage Converter PWB Assembly A3A1 and EMI Filter Assembly A3A2.

(2) The major function of the Multivoltage Converter Assembly is to power the low-level circuitry in the Remote Control. To do this, the assembly develops ±15 Vdc and +5 Vdc from a +10 to +32 Vdc input, using a push-pull switching power supply and a series-pass switching power supply. Refer to simplified diagram FO-4 and schematic diagram for the following discussion.

b. Basic Switching Power Supply Operation. The power supply used in this equipment is a switching regulator. In basic operation, the input voltage is passed to the output filter as a train of pulses at a fixed repetition rate but with a controllable duty cycle. The duty cycle of the pulses is determined by the amount of error in the output voltage. The output filter network has a choke input and a flyback diode that allows the current through the choke to continue during the off-time of the pass transistors. The pulses are thus integrated to yield a dc voltage at the output of the filter. This output voltage is compared to a stable reference in the regulator. The result of the comparison controls the duty cycle of the pulses and thus controls the output voltage.

c. ±15 V Supply. The +10 to +32 Vdc input is first passed through EMI Filter FL1, a subassembly of the Multivoltage Converter Assembly. The output of FL1 then passes through choke L1 and is applied to Voltage Stabilizer Q1.

(1) Voltage Stabilizer Q1. Voltage Stabilizer Q1 maintains the voltage at the input of U1 and the driver stage (T1) at approximately +12 V. Once the power supply starts running, +15 V is fed back through CR1 to the emitter of Q1, so that the power supply runs on its own output. The emitter of Q1 is connected to the CA and CB outputs of Pulse-Width Modulating Regulator U1.

(2) Pulse-Width Modulating Regulator U1.

(a) The ±15 V output is developed by a push-pull switching regulator, driven by Pulse-Width Modulating Regulator U1. U1 is a regulating pulse-

width modulator containing all control circuitry for the switching regulator power supply. Included in the 16-pin dual-in-line package is the voltage reference, error amplifier, oscillator, pulse-width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. Refer to figure 5-3. The following discussion describes elements within the regulator chip, since this information is required for an understanding of the external circuit.

(b) The oscillator in U1 uses an external resistor (R22 at pin 6) to establish a constant charging current into an external capacitor (C12 at pin 7). This provides a linear ramp voltage on the capacitor which is used as a reference for the comparator. The discharge time of C12 determines the pulse-width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse for both outputs. The oscillator period, in microseconds, is approximately t=(0.8)RC, where R is in ohms and C is in microfarads.

(c) Within U1, a linear regulator provides a constant +5 volt output with input voltage variations of +8 to +40 volts. It is internally compensated and short-circuit protected. It is used both to generate a reference voltage and as the regulated source for all the internal timing and controlling circuitry.

(d) The error amplifier circuit is a simple, trans-conductance amplifier with differential input. The gain of this amplifier is nominally 10,000 but is reduced by a feedback network or by shunting the output to ground. Phase response of the amplifier is compensated by an external RC combination at pin 9. Since the error amplifier is powered by the internal +5 volt reference voltage, the acceptable common-mode input voltage range is restricted to +1.8 to +3.4 volts. This means the reference must be divided down to be compatible with the amplifier input.

(e) The two outputs of U1 (CA at pin 12 and CB at pin 13) alternately drive transistors Q3 and Q4 to produce an ac current through the center-tapped primary of Driver Transformer T1. A bias current from the filtered dc line input is fed to the center tap via Voltage Stabilizer Q1. Bias current begins to turn the appropriate transistor on before the collector current builds up. When no drive is required, both Q3 and Q4 are on, shorting out T1.

(3) Driver Transformer T1. Driver Transformer T1 provides the transition from the low-level drive impedence to the transistor base impedence. T1 uses collector current feedback, with one turn of the secondary at the collector of Q8 and one turn at the collector of Q9, to provide a base current that is proportional to the collector current.

(4) Current Limit T2. The two primary leads of T1 are fed through transformer-coupled Current Limit T2. The outputs of T2 are then rectified by diodes CR10 and CR11. The network composed of Q7, R40, C13, R39, C14, C39, and R44 provides the correct loop compensation and current limit input to pin 4 of U1.

(5) Power Transformer T3. Transistors Q8 and Q9 alternately drive center-tapped Power Transformer T3. The leads of each secondary coil are fed to two diode networks, one for the +15 V output (CR12) and one for the - 15 V output (CR16 and CR17). The output of CR12 is then filtered by L2 and C19. The -15 V line is filtered by L3 and C20. Both lines are then passed through EMI Filter FL1 which provides outputs to other assemblies in the Remote Control.

(6) Output Voltage Feedback. The +15 V output is sampled at the input to FL1 and fed back through a voltage divider; the feedback voltage can be adjusted with potentiometer R4. The divided down feedback voltage is the input to U1 at pin 1. In U1, the feedback voltage is compared to a reference voltage. The error is then used to determine the pulse-width of outputs at pins 12 and 13. The pulse width controls the voltage level on the +15 V (and consequently -15 V) line.

(7) Under-Voltage/Over-Voltage Protection AR1. Voltage Comparators AR1-A and AR1-B provide under-voltage and over-voltage protection. AR1 shuts down U1 when line voltage is outside the range of +9 to +35 V. A stable +5 V from U1-16 is divided down by the voltage divider composed of R24, R28, and R32 and used as reference to the comparators.

(8) Soft-Start Switch Q6. Soft-Start Switch Q6 is driven by AR1-A through common-base amplifier Q12.

d. <u>+5 V Supply.</u> The filtered +10 to +32 Vdc input line also passes from choke L1 to circuitry that develops the +5 V supply. The +5 V supply is generated by a series-pass switching regulator, which is driven by Pulse- Width Modulating Regulator U2.

(1) Pulse-Width Modulating Regulator U2. Figure 5-4 is a simplified block diagram of U2. The output of U2 (pin 7) switches high and low, generating a pulse at the base of Q11 (via Q13). The frequency of this pulse is determined by R51 and C25 (at pin U2-5). Circuitry in U2 compares feedback from the +5 V output line of the power supply to a reference voltage. U2 then adjusts the pulse-width at pin 7 according to the result of this comparison. The pulse-width determines the voltage level on the +5 V line.

(2) Current Transformer T4. When Q11 is enabled by U2 (via Q13), it drives Q10. Q10 and Q11 are also driven by Current Drive Transformer T4, which senses the collector current and provides a proportional base current. The output of the Current Drive Transformer section of T4 is connected to the primary of Current Limit Transformer T4.

(3) Current Limit Transformer T4. The one-turn primary of Current Limit T4 is located at the collector leads of Q10 and Q11, to sense output current. The secondary of T4 is connected to current sense input U2-6 through the network of CR22, R49, R50, and C24. When the input at U2-6 begins to exceed the limit, U2 decreases the pulse-width of the output at U2-7.

(4) +5 V Output and Feedback. From the primary of T4, the pulse from Q10 and Q11 is filtered by L4 and C21 and passed through EMI Filter FL1. +5 V is then distributed from FL1 to other areas in the Remote Control. A sample of the output is taken at the input to FL1 and fed back to U2. Before it is input to U2, this sample is divided down by a voltage divider that is adjustable with potentiometer R61. The divided down sample is then returned to feedback input, pin 3, of U2. This feedback voltage is compared to an internal reference voltage. The amount of error in the feedback determines the pulse width at output pin 7, which, in turn, controls the voltage level on the +5 V line.

(5) Under-Voltage/ Over-Voltage Protection Q14. The +5 V switching power supply uses the same under-voltage/ over-voltage protection circuit as the ±15 V switching power supply. The output at the collector of Q6 controls the bias of Q14 via CR24 and R71. During shut-down, Soft-Start Switch Q6 is biased on, which biases Q14 on. Q14 pulls pin U2-4 to ground, which shuts down U2.

5-17 AUDIO INTERFACE PWB ASSEMBLY A4. This manual portion describes the Audio Interface PWB as an individual assembly. Section I of this chapter describes the function of the Audio Interface PWB in relation to overall Remote Control operation. The following references apply for the detailed discussion that follows:

a. Schematic Diagram	Depot Manual
b. Parts List	Depot Manual
c. Component Layout	Depot Manual
d. Overall Interconnection	Depot Manual
e. Remote Control Simplified Block Diagram	Figure 5-1

5-18. OVERALL AUDIO INTERFACE PWB FUNCTION. The purpose of the Audio Interface PWB is to provide an interface between the Remote Control rear panel terminal strip TB1, and the audio functions associated with the Audio/Microprocessor PWB Assembly. TB1 is used for connection to telephone lines (patch) or the 100 Watt Transceiver (line). Additional TB1 connections include a push-to-talk keyline input, AGC Monitor output, and signal ground. The Audio Interface PWB hybrid transformers convert separate Remote Control receive and transmit audio to and from a 2-wire circuit. The audio connections to TB1 may be from 2-wire or 4-wire circuits.

5-19. TERMINAL CONNECTIONS FOR 4-WIRE AUDIO. When 4-wire connections are made, the following terminals are used:

TB1-1	Patch Audio Input - Balanced
TB1-2	Patch Audio Input - Balanced
TB1-3	Patch Audio Output - Balanced
TB1-4	Patch Audio Output - Balanced
TB1-5	Line Audio Input - Balanced
TB1-6	Line Audio Input - Balanced
TB1-7	Line Audio Output - Balanced
TB1-8	Line Audio Output - Balanced

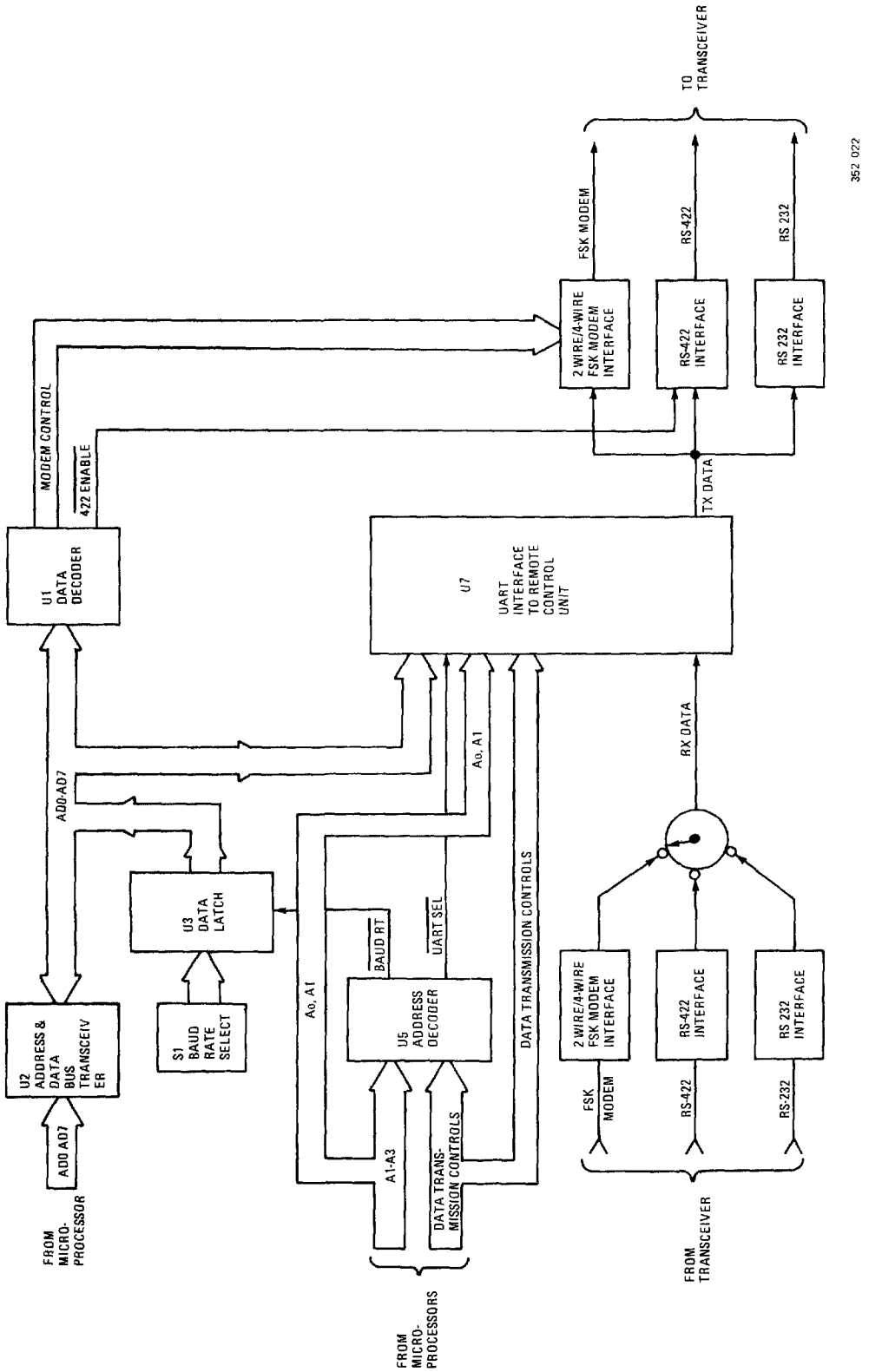


Figure 5-5. Simplified Remote Control Interface Assembly

5-20 TERMINAL CONNECTIONS FOR 2-WIRE AUDIO. When 2-wire connections are made to TB1, the following terminals are used:

TB1-1	(Not Used)
TB1-2	Patch Audio Input/Output -Balanced
TB1-3	Patch Audio Input/Output -Balanced
TB1-4	(Not Used)
TB1-5	(Not Used)
TB1-6	Line Audio Input/Output - Balanced
TB1-7	Line Audio Input/Output -Balanced
TB1-8	(Not Used)

5-21. BALANCED AUDIO. When input audio connections are from a 2-wire circuit, hybrid transformers are used to convert the input into a 4-wire circuit. The patch audio circuit uses transformers T1 and T2 with switch S1; T3 and T4 and switch S2 are used for line audio. Switches S1/S2 must be placed in the 2-wire or 4-wire position to match the audio connections. The hybrid balance is adjusted with R1/R5 to prevent cross-talk between the transmit and receive audio signals.

5-22. UNBALANCED AUDIO. In addition to the 2-wire/4-wire conversion, T1-T4 convert the balanced audio connections at TB1 into 600 ohm unbalanced audio for use in the Remote Control.

5-23. REMOTE CONTROL INTERFACE PWB ASSEMBLY A1A19. The following references apply for the detailed discussion that follows:

a. Simplified Remote Control Interface Assembly	Figure 5-5
b. Remote Control Interface PWB Assembly Schematic Diagram	Depot Manual
c. Parts List	Depot Manual
d. Component Layout	Depot Manual
e. Overall Interconnection	Depot Manual
f. Remote Control Simplified Block Diagram	Figure 5-1

5-24. OVERALL REMOTE CONTROL INTERFACE PWB ASSEMBLY FUNCTION. The Remote Control Interface PWB Assembly must be installed in the 100 Watt Transceiver when a Remote Control is used. This assembly provides the interface between the Remote Control microprocessor and the 100 Watt Transceiver microprocessor. The circuitry on the Remote Control Interface PWB Assembly includes FSK Modem, RS 422, and RS 232 interfaces, as well as BAUD rate control.

a. Address and Data Transfer.

(1) UART U7.

(a) UART U7 tranfers data between address and data bus AD0 through AD7 and the data interface circuitry to the Remote Control. The UART is enabled by address lines A1 through A3 from the 100 Watt Transceiver microprocessor. These lines are decoded by Address Decoder U5 (and AND gate U17A) to produce the low-true UART SEL signal. When UART SEL is low, U7 is selected.

(b) The serial receive data is written into the UART data register from RXD (Receive Data) input pin 3. Serial transmit data is written out of the UART data register at TXD (Transmit Data) output pin 19. The DT/R (Data Transmit/Receive) signal configures the UART to write to or read from a data register. The data register is selected by address lines A0 and A1 from the 100 Watt Transceiver microprocessor.

(c) When the receive data holding register has a character to be input to the microprocessor, the UART places a low on the RX RDY (Receive Ready) line at output pin U7-14. When the character has been read, RX RDY goes high.

(d) When the transmit data holding register is ready to accept a character from the microprocessor, the UART places a low on the TX RDY (Transmit Ready) line at output pin U7-15. When the character is loaded, this line goes high.

(e) When the last character loaded by the microprocessor has been serialized, the UART sends a low-true Tx EMT (Transmit Empty) signal to the 100 Watt Transceiver microprocessor.

(f) The clock to U7 and U12 (at pin 20) is produced by 4.9152 MHz crystal oscillator Y1.

(2) Address and Data Bus Transceiver U2. Address and Data Bus Transceiver U2 is a bidirectional buffer, which allows transfer of address and data bits AD0 through AD7 between the 100 Watt Transceiver microprocessor and the address and data bus.

(3) Data Buffer U3. Data Buffer U3 presents BAUD rate selection from BAUD Rate Select Switch S1 onto the address and data bus. U3 also connects the Tx EMT and DCD signals onto the bus. U3 is enabled by the low- true BAUD RT signal at the output of Address Decoder U5.

b. Data Interface. The Remote Control Interface PWB Assembly provides the three types of interfaces used on the Audio/Microprocessor PWB Assembly: FSK Modem (Bell 103 Standard), RS 422, and RS 232.

(1) Interface Select Switch S2. Interface Select Switch S2 is positioned to select either the RS 232, RS 422, or FSK Modem interface for receive data. The TXD (Transmit Data) position is used to loop back the receive data into the transmit path for testing purposes.

(2) FSK Modem Interface.

(a) Two/Four-Wire Operation Switch S5 configures the FSK Modem interface for either two-wire or four-wire operation. In two-wire operation, transformer T2 handles both transmit and receive data. In four- wire operation, T2 handles the transmit data, and transformer T1 handles the receive data.

(b) FSK Modem U9.

1 300 BAUD FSK Modem U9 has filter and modem circuitry to convert serial input data to the audio tones required for FSK Modem signaling. Transmit data from the microprocessor (via Address and Data Bus Transceiver U2 and UART U7) is input at pin U9-10 and output at pin U9-16 as audio FSK tones to op-amp input U18-2. This op-amp presents the generated FSK transmit frequencies to T2, which then outputs the FSK data to the Remote Control via connector J1.

2 Receive audio FSK data from either T2 (two-wire operation) or T1 (four-wire operation) is input to op-amp U18B pin 6, which then presents the receive audio FSK data to pin 15 of FSK Modem U9. U9 converts this data to serial data and sends it (via pin U9-4) to two series- connected NOR gates (U15A, U15B), along with the DCD (Data Carrier Detect) signal from pin U9-2. The DCD signal at pin U9-2 goes low when a valid carrier frequency is detected on the incoming receive audio FSK data. The DCD signal then allows receive data to pass through U15, from which it is routed (via S2) to the RXD (Receive Data) input (pin 3) on UART U7. The receive data is then routed via the data bus to the 100 Watt Transceiver microprocessor.

3 A MODEM BIT command may be generated at the 100 Watt Transceiver microprocessor and input to pin 1 of U9. The MODEM BIT command configures U9 to loop transmit data back internally to the FSK receive data path. This feature tests operation of FSK Modem U9 when Interface Select Switch S2 is in the FSK position.

(3) RS 422.

(a) Transmit data from the 100 Watt Transceiver microprocessor is input to U10 for conversion to bipolar RS 422 data at outputs J1-10 (+) and J1-13 (-).

(b) RS 422 receive data enters the Remote Control Interface PWB Assembly at pins J1-20 (+) and J1-21 (-). These lines are input to pins 6 and 7 of U11. The output of U11 is then relayed to the RXD input to UART U7 via S2.

(4) RS 232. Transmit data for the RS 232 output is inverted by line driver U14A and output at J1-22. RS 232 receive data is inverted by line receiver U13A and relayed to the RXD input to UART U7 via S2.

c. Voltage Regulation VR1, VR2, VR3, and VR4. Voltage Regulator VR1 develops a regulated -5V from +15 V. Voltage Regulator VR2 supplies a regulated +7 V to pin 14 of U14, and VR3 supplies a regulated -7 V to pin 1 of U14. Voltage Regulator VR4 supplies +12 V to FSK Modem U9.

NOTE

VR2 and VR3 are normally not installed. In this case, the +15 V and -15 V inputs are connected to the regulator's output node after passing through a diode network that lowers their potential from 15 V to 13.8 V.